

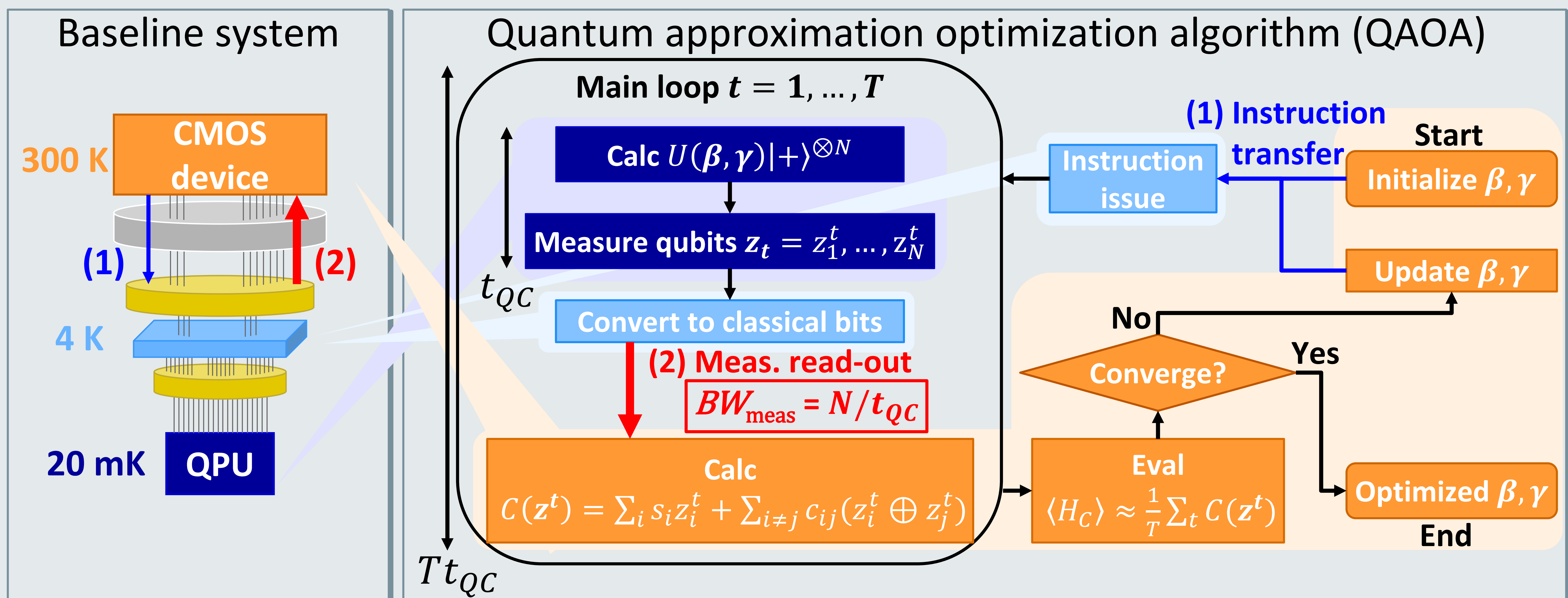
Inter-temperature Bandwidth Reduction in Cryogenic QAOA machines

超伝導量子計算機のシステムレベル最適化に向けて～QAOAを対象とした場合～

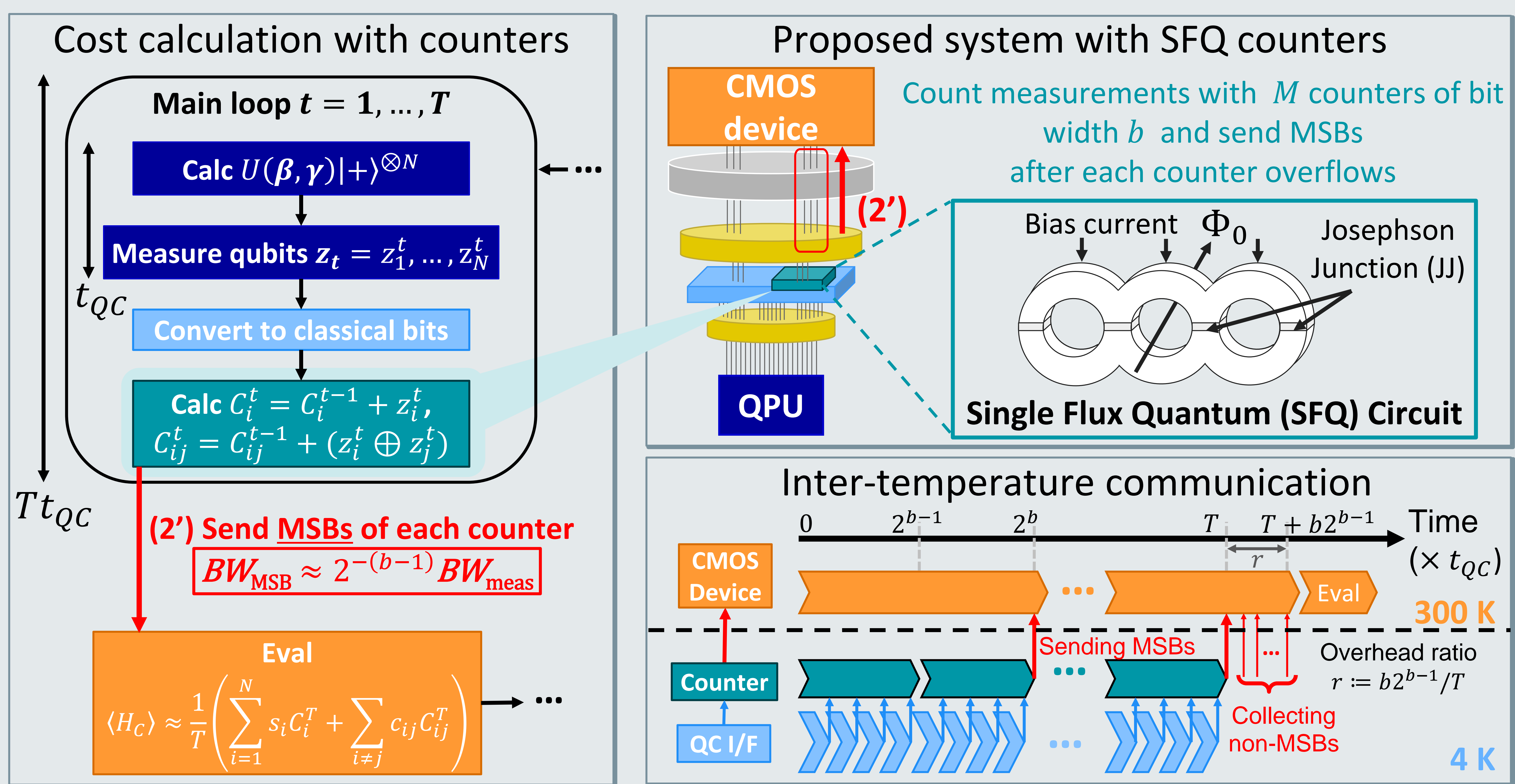
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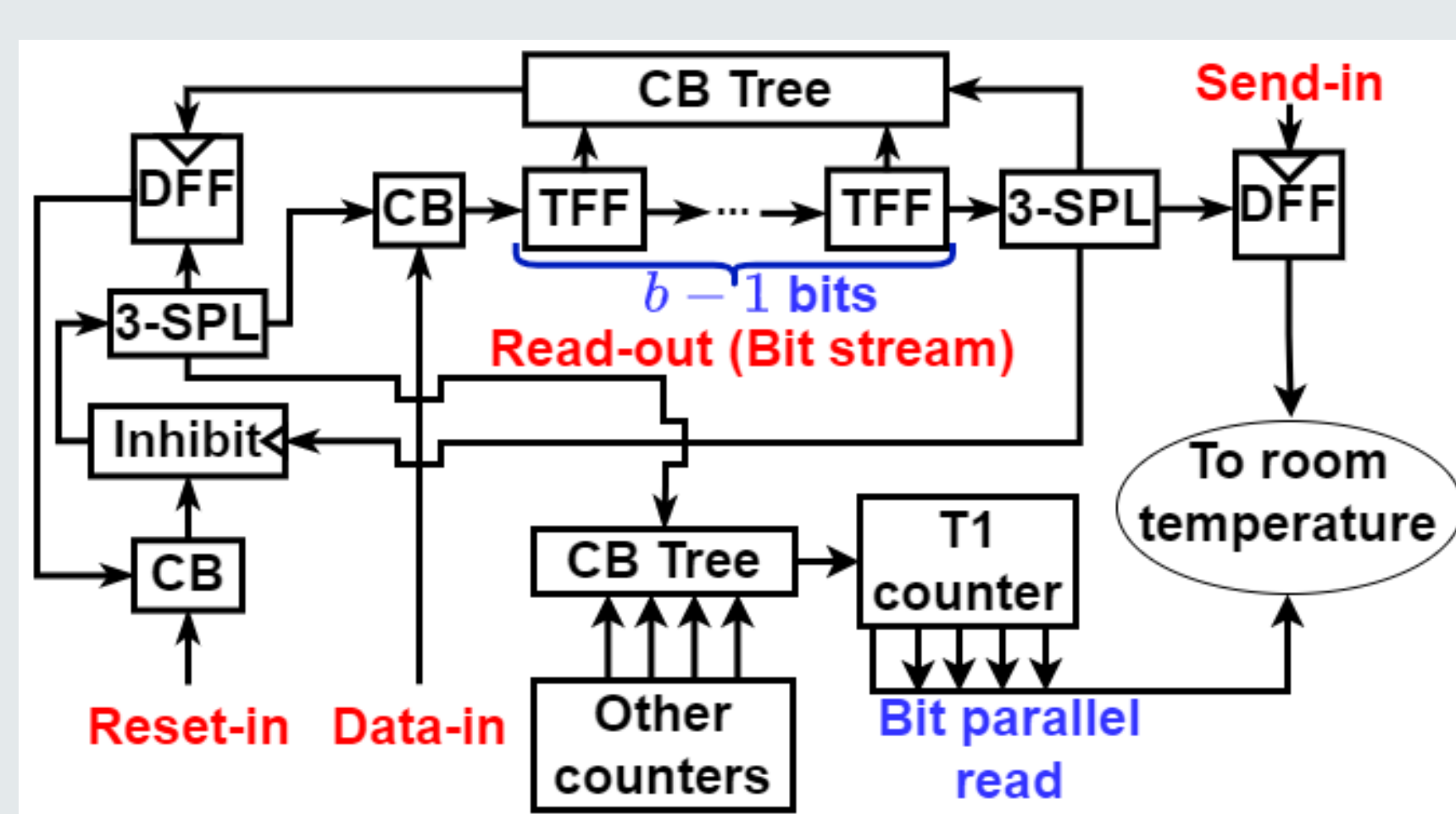
QAOA execution on a superconducting quantum computer



Counter-based architecture for measurement bandwidth reduction

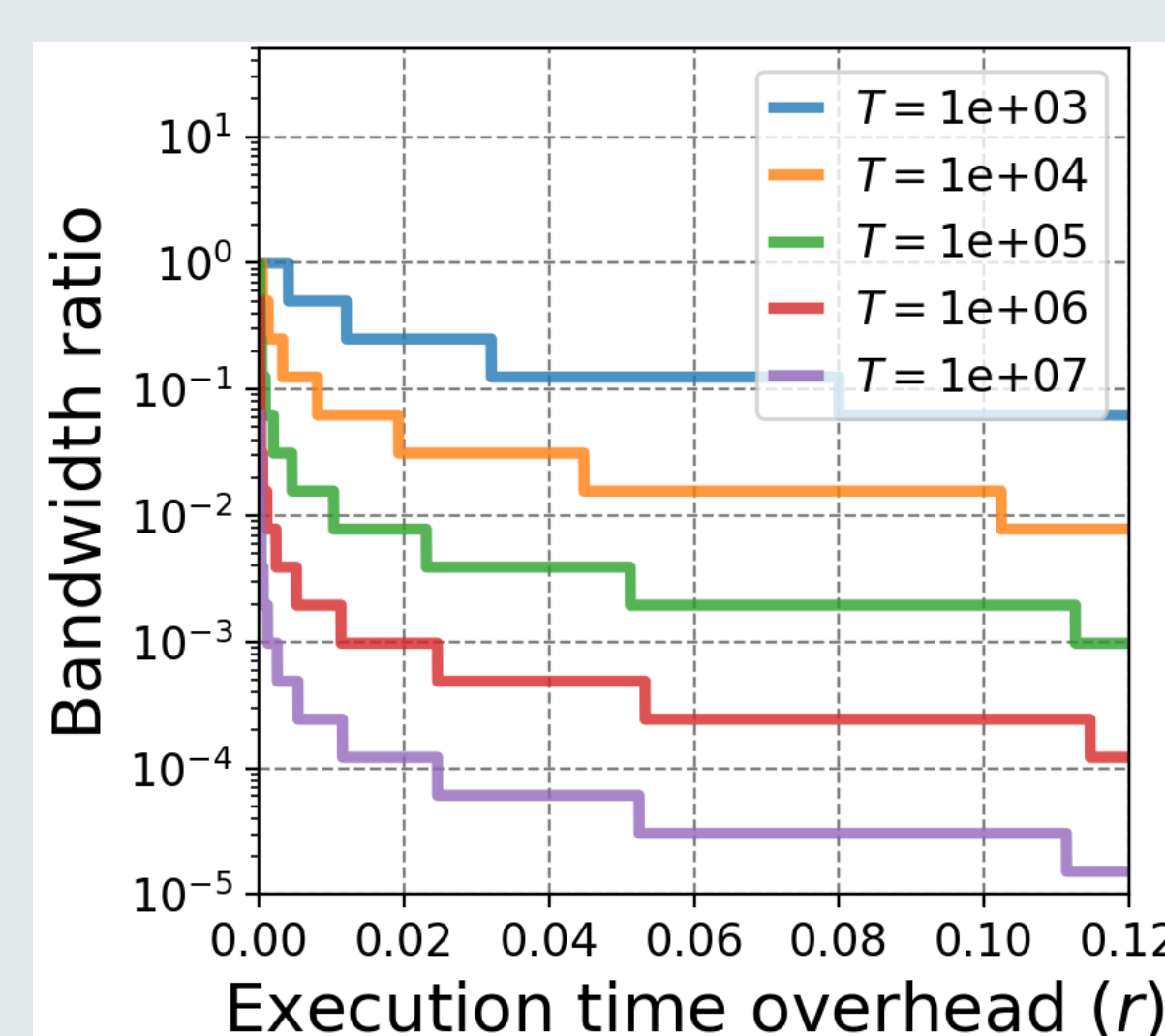


Circuit design

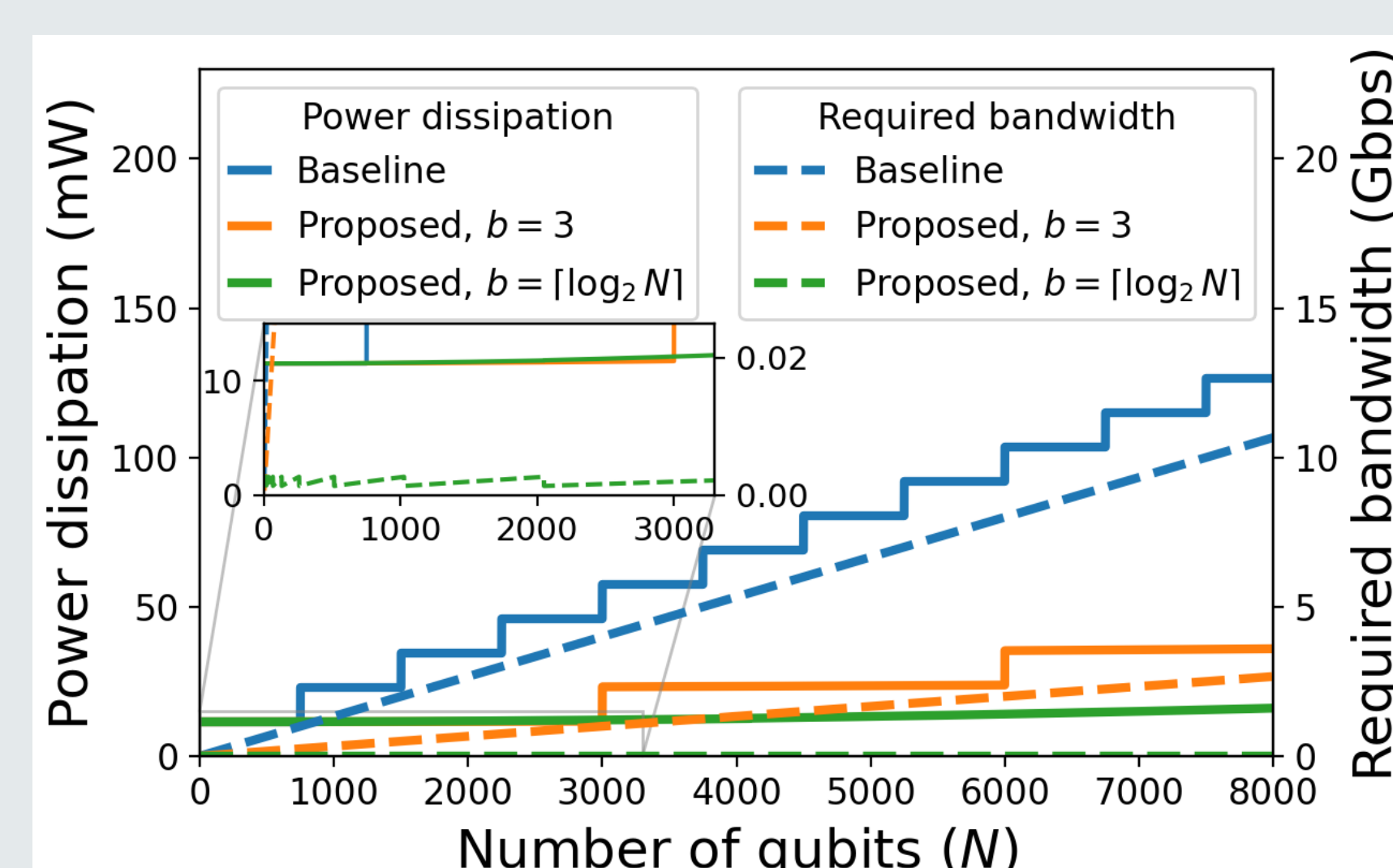


JJs: $11b+31$ Power: $9.71b+16.8$ (pW)

Evaluation



Bandwidth reduction to time overhead r



Power dissipations

Configuration

Cable:

- Heat inflow: 1.0 mW
- Peripheral : 10.5 mW
- Bandwidth : 1 Gbps

SFQ counter:

- Power: $9.71b+16.8$ (pW)
- # : $N(N+1)/2$

Required bandwidth (Gbps)

(heat inflow and power consumption)

Summary

Our method reduced the communication during QAOA by transferring the MSB of SFQ counters. Our architecture achieved exponential bandwidth reduction and decreased cables power dissipation in a cryogenic environment with the negligible power overhead.