Online surface code decoder with a superconducting circuit

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- Career
  - 2022.3: Ph.D. in Information Sci. and Tech. @ University of Tokyo
    - Supervisors: Masaaki Kondo (Keio Univ., R-CCS), Hiroshi Nakamura
    - Thesis: Online Quantum Error Correction Using a Superconducting Circuit
  - 2022.5 to 2023.2: Guest researcher @ Technical University Munich
  - 2023.4 to Present: SPDR @ RIKEN Center for Quantum Computing
- Research interest
  - Computer architecture
  - Quantum error correction
  - Cryogenic computing

My first and last beer in Germany

Summary of this talk

- Decoding surface code is reduced to graph matching problem
- A practical decoder should be **accurate, fast, and scalable**
- For superconducting QCs, decoder also should be **power efficient** to be operated in **a cryogenic environment**
- Our solution: **online decoder** with **superconducting digital circuit**
  - QECOOL: Online decoder with superconducting circuits (DAC'21, arXiv:2103.14209)
  - QULAIS: Extension of QECOOL for logical operation with lattice surgery (HPCA'22)
  - NEO-QEC: Extension of QECOOL/QULATIS with binarized NN for better accuracy (arXiv:2208.05758)

Outline

- Introduction
  - Superconducting quantum computer
  - Quantum error correction with surface code
- Requirements for a practical decoder
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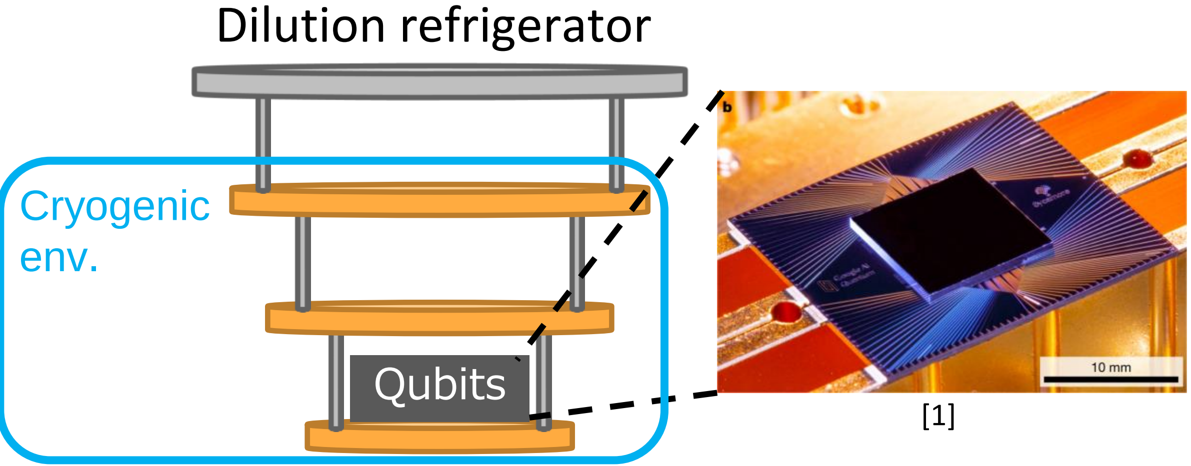
Superconducting quantum computer (QC)



[1]

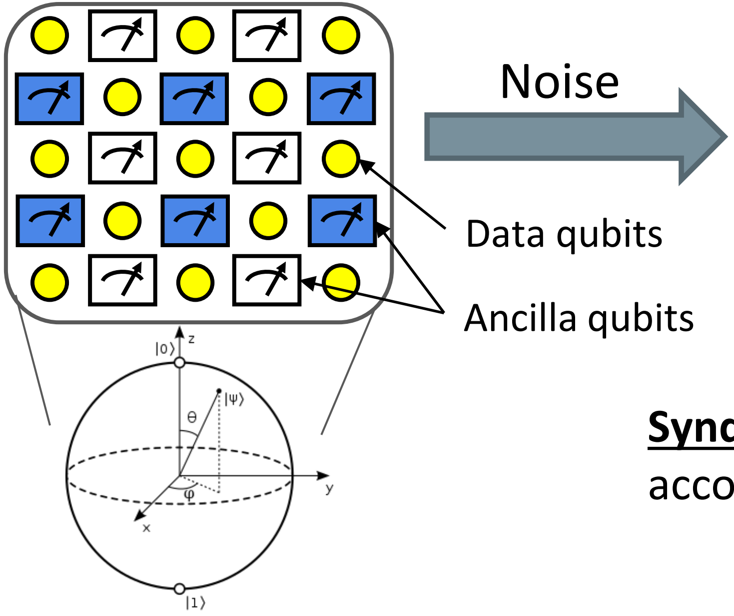
- # of qubits: around 100
- Error rate: **<u>1%</u>**
- Noisy Intermediate Scale Quantum (**<u>NISQ</u>**) device

- Superconducting qubit: one of the most promising qubit implementation
  - Operate only at cryogenic environment (~20 mK)
- Qubits have very low error tolerance
  - **<u>Quantum error correction (QEC) code</u>**

[1] Frank Arute, Kunal Arya, Ryan Babbush, et al., Quantum supremacy using a programmable superconducting processor, Nature 574, 505–510 (2019).

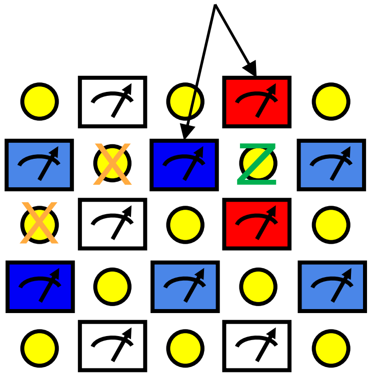
Surface code

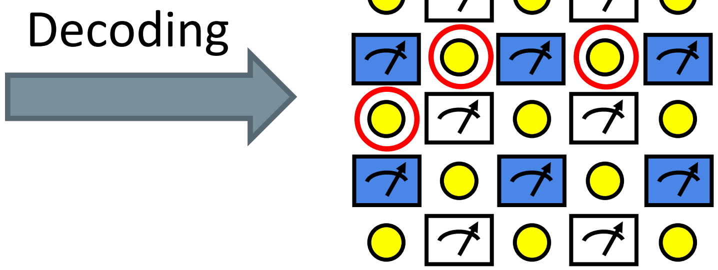
Surface code
(Code distance $d = 3$)



Logical qubit

Hot syndromes

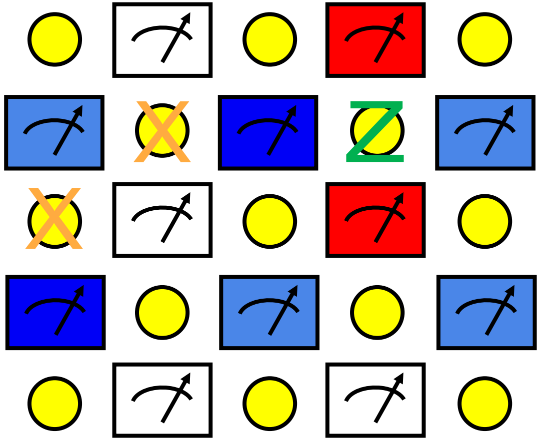


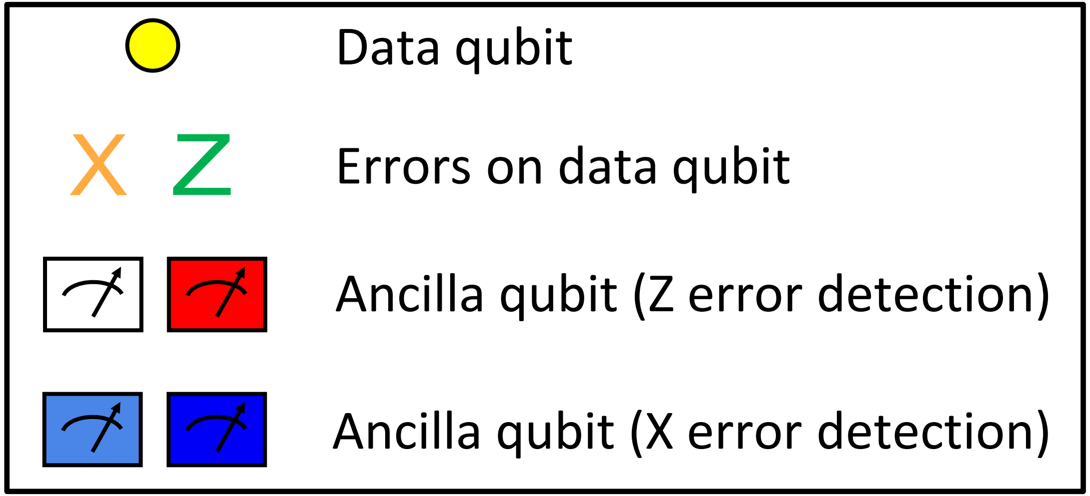


Syndromes change according to errors

Decoding SC is specifying most likely errors from **hot syndromes**, and reduced to **graph matching problem**

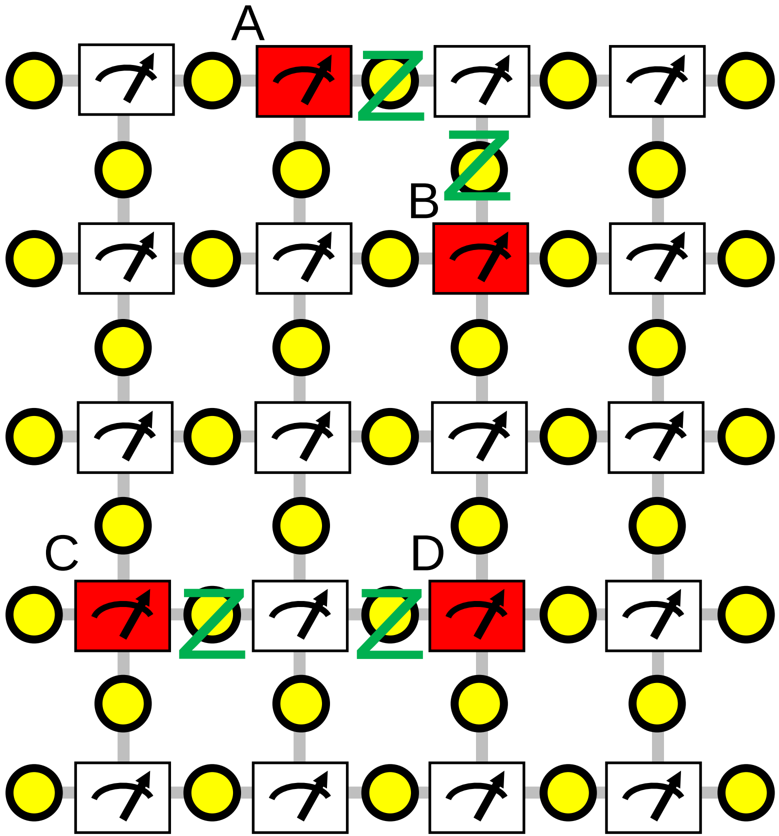
Function of surface code





- Each ancilla qubit is used for error parity detection of neighboring data qubits
  - Endpoints of error chains are expected to be **hot syndromes**
- Errors on data qubit can be detected without direct measurement

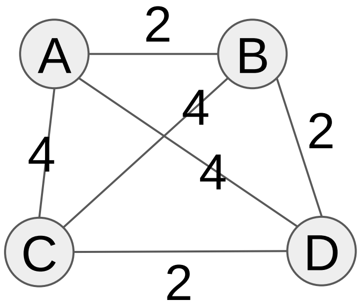
Decoding surface code



Assumption

- *X* and *Z* errors can be decoded independently
- Shorter error chains are likely to occur

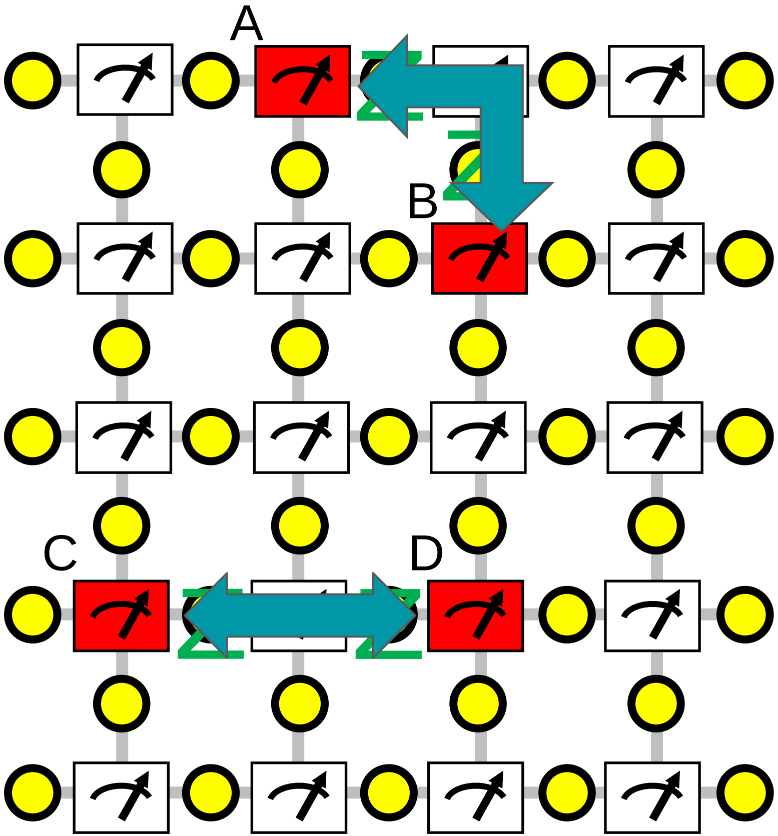
Minimum Weight Perfect Matching (MWPM)



V: Hot syndromes
W_e: Manhattan distance

Exact solution: **Blossom algorithm (*O*(n³))**

Decoding surface code



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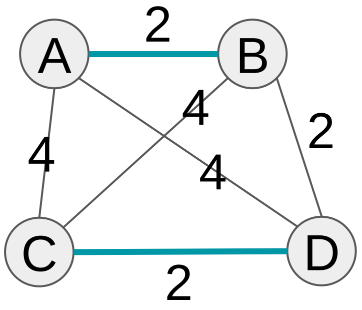
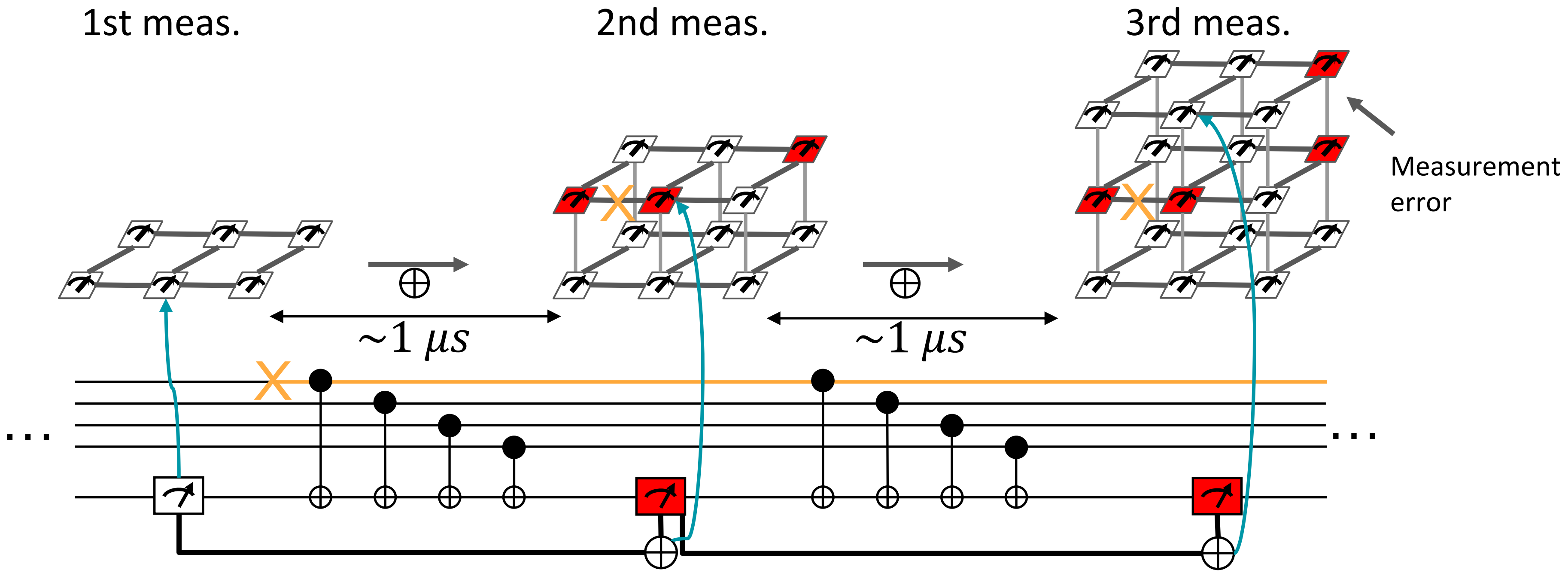
Minimum Weight Perfect Matching (MWPM)



V: Hot syndromes
W_e: Manhattan distance

Exact solution: **<u>Blossom algorithm (O(n³))</u>**

Measurement error on ancilla qubit



- If ancilla qubit measurement is susceptible to read errors, multiple measurement processes are required
  - For every new measurement, the new syndrome is **XORed** with the latest value

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Requirements for a practical decoder

Requirements

1. Power consumption
   - Decoder must operate in **a cryogenic environment** with limited power budget
2. Latency
   - Slow decoding leads to **accumulation of errors** and **slow quantum computation**
3. Functionality
   - Decoder must protect not only single qubit but also **logical operations**
4. Accuracy
   - Decoder must have a **high error threshold**

QECOOL, DAC'21

QULATIS, HPCA'22

NEO-QEC, arXiv:2208.05758

Our solutions

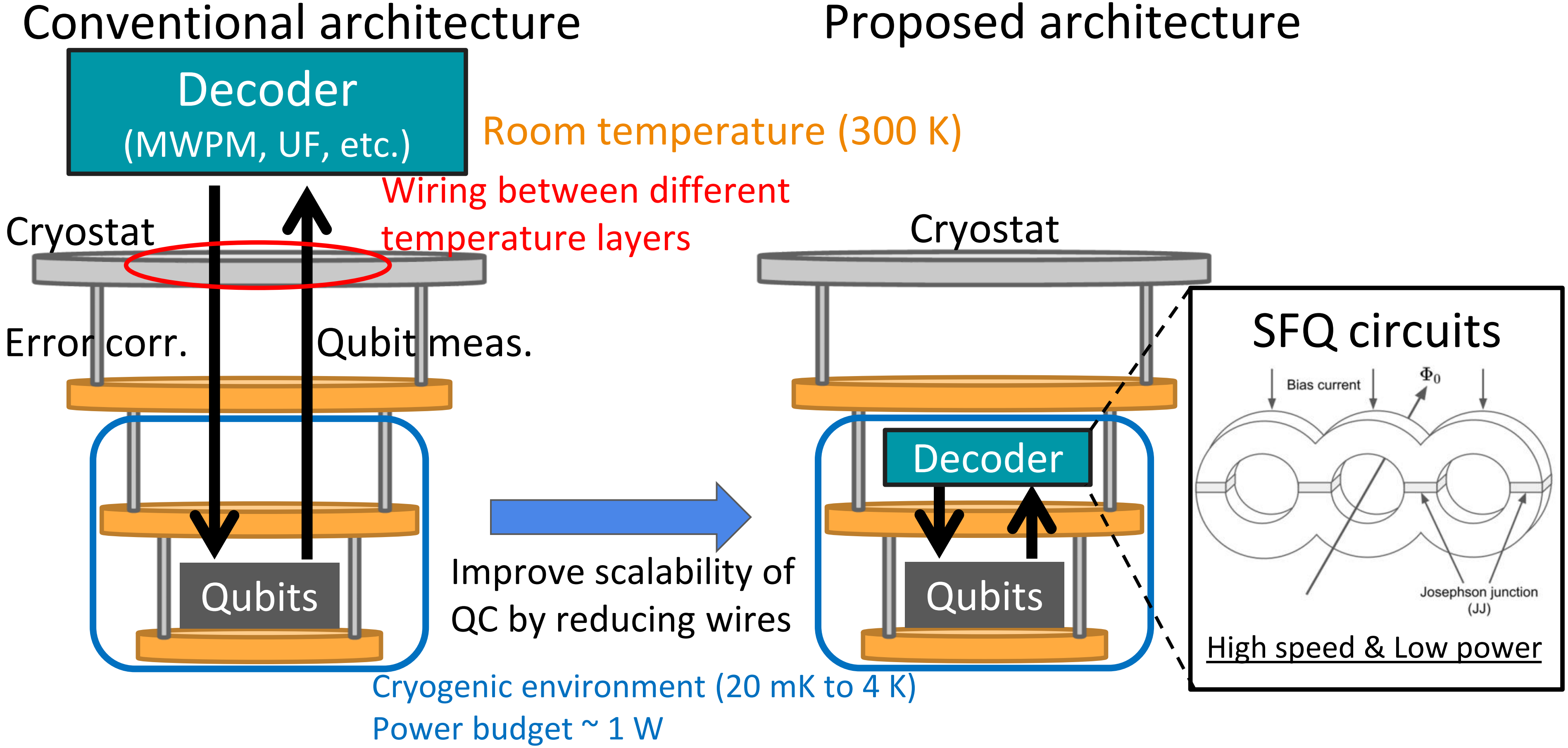
Superconducting digital circuits

Online-QEC manner

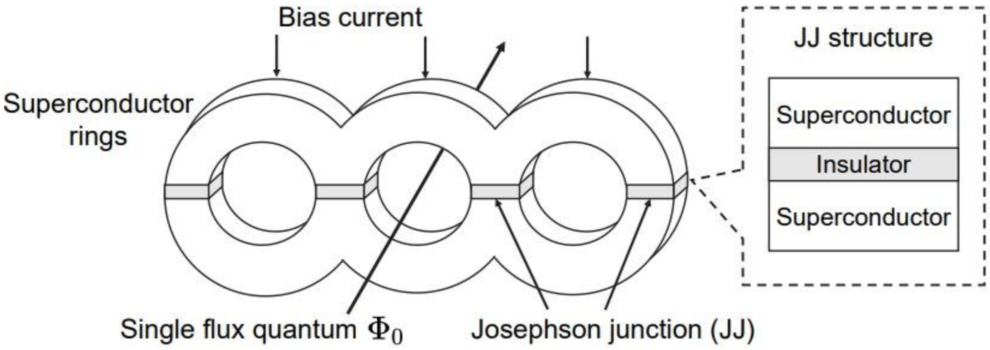
Binarized neural network

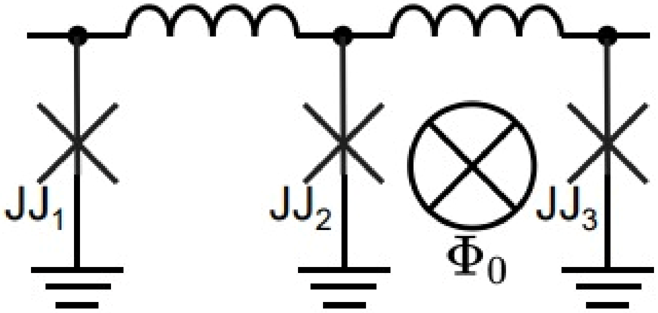
QEC architecture for supercond. QCs

Req 1. Power



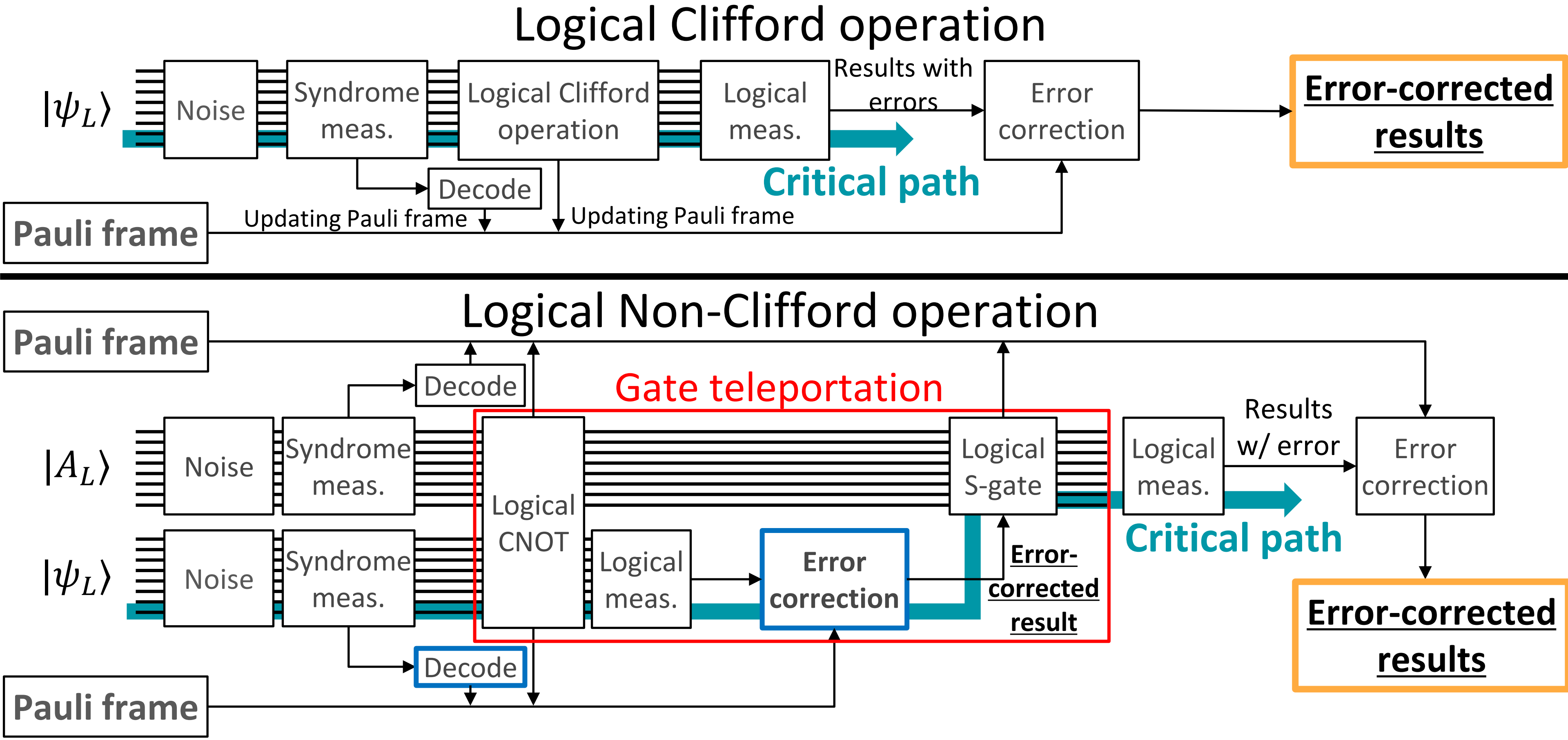
Single flux quantum (SFQ) logic



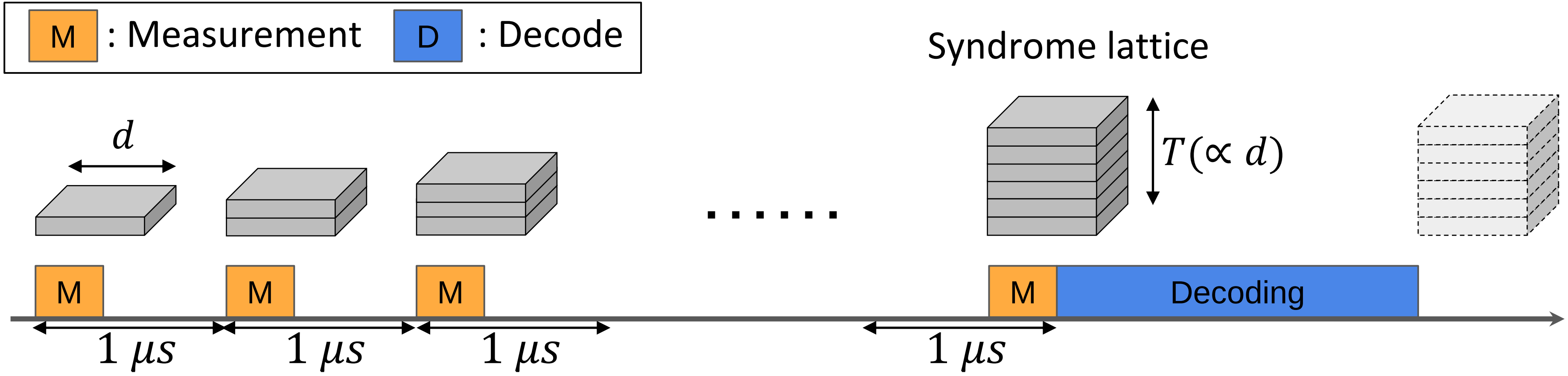


- Absence (presence) of flux quanta within the ring represents digital ‘0’ (‘1’)
- Operates only in a cryogenic environment (~ 4 K)
- High speed and low latency compared to CMOS circuits
- Limitation: Large amount of RAM is expensive
  - -> Conventional decoders such as MWPM are not implementable with SFQ

Impact of decoding latency



Why is MWPM not practical?

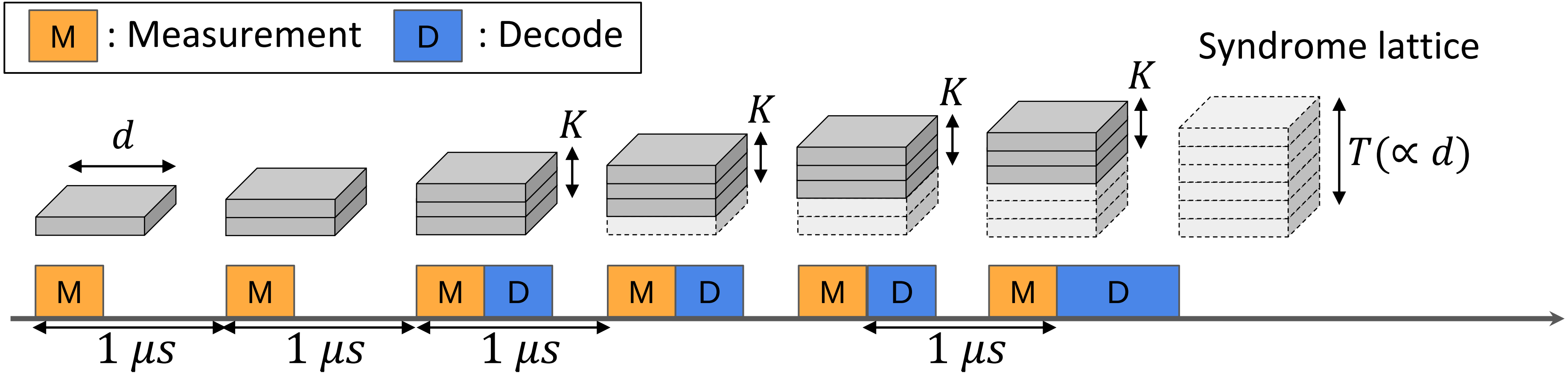


Measurement and decoding processes with the MWPM decoder

Batch-QEC manner

+ Accurate decoding
− Slow decoding
− $O(Td^2)$ bits of storage

Our solution: Online-QEC manner



Measurement and decoding processes with a practical decoder

Online-QEC manner

− Degradation of decoding accuracy

+ Fast decoding

+ $O(Kd^2)$ bits of storage

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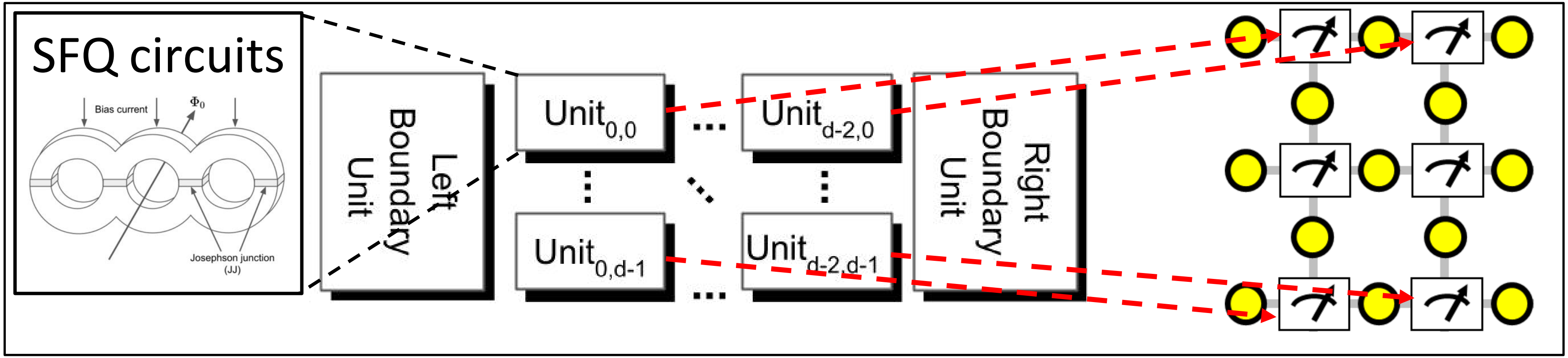
QECOOL

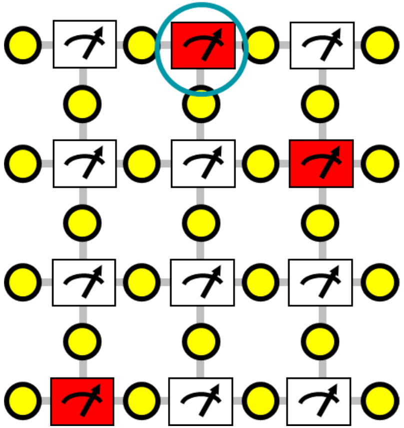


Architecture overview of QECOOL decoder

- Quantum Error COrrection by On-Line decoding algorithm
- **A distributed architecture** without large amount of RAM
  - Multiple processing elements (***Units***) corresponding one-to-one with ancilla qubits
  - Matching problems are solved by signal propagation among Units

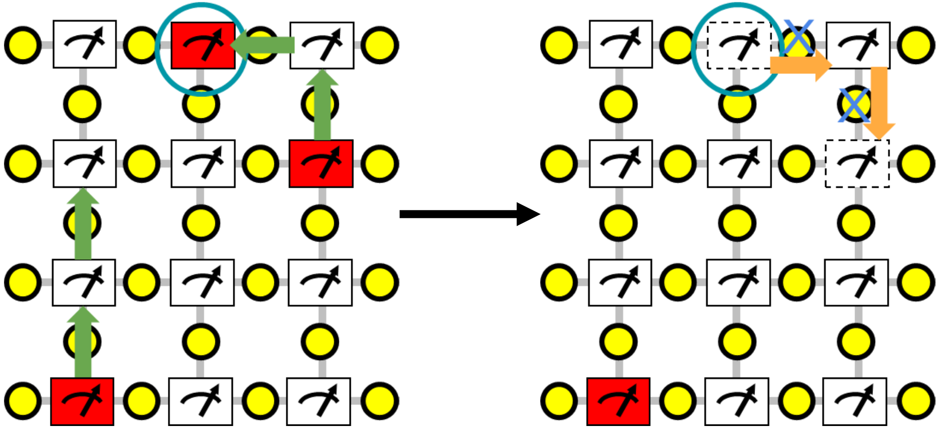
Overview of QECOOL algorithm

Step 1



Determine the starting point for finding a hot syndrome pair

Step 2

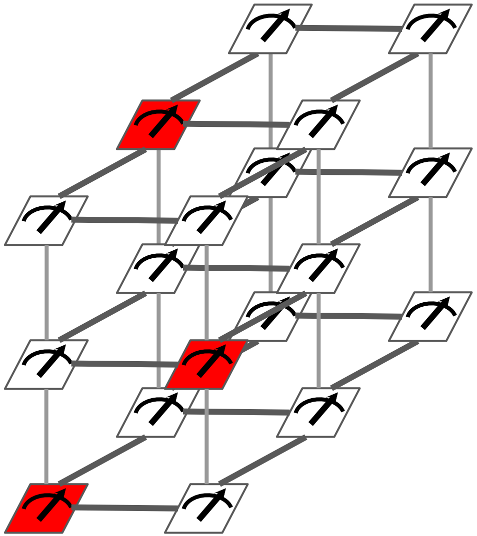


Perform **nearest neighbor search** using two types of signals among Units

Based on a **greedy graph matching algorithm**

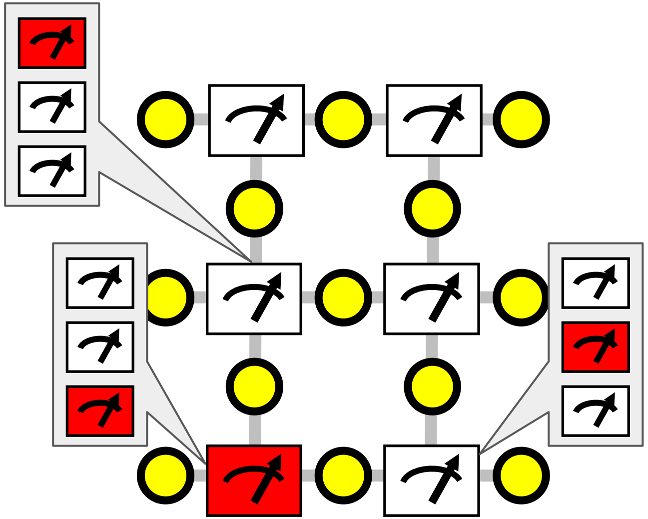
$O(n^2)$, approximation degree 1/2

Matching problem on a 3-D lattice



3-D syndrome lattice

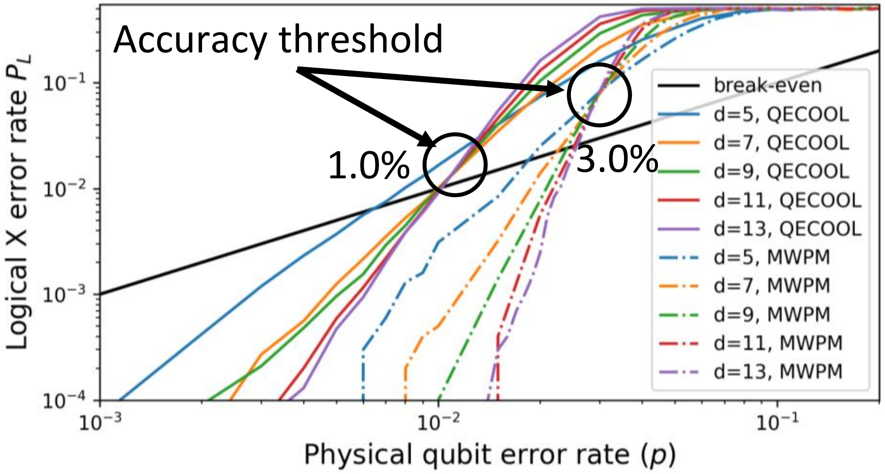
Map 3-D lattice to Units on 2-D grid

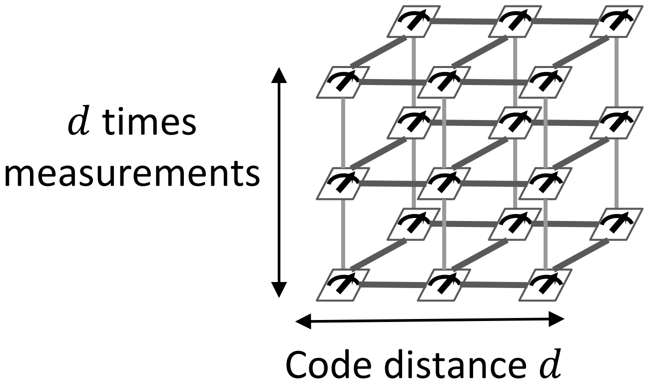


Units with $O(K)$ memory

- Each Unit has a $O(K)$ buffer to store multiple syndrome values
- Almost the same procedure as in case of 2-D lattice

Decoding performance of QECOOL





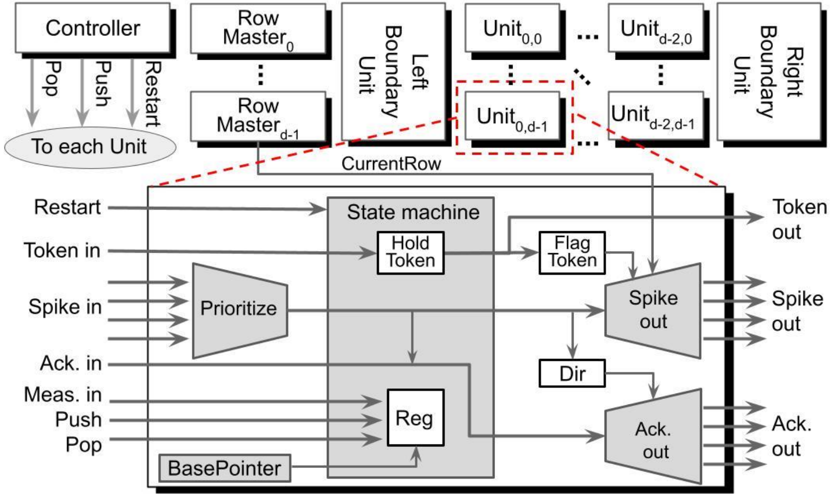
Target lattice shape

Experimental condition

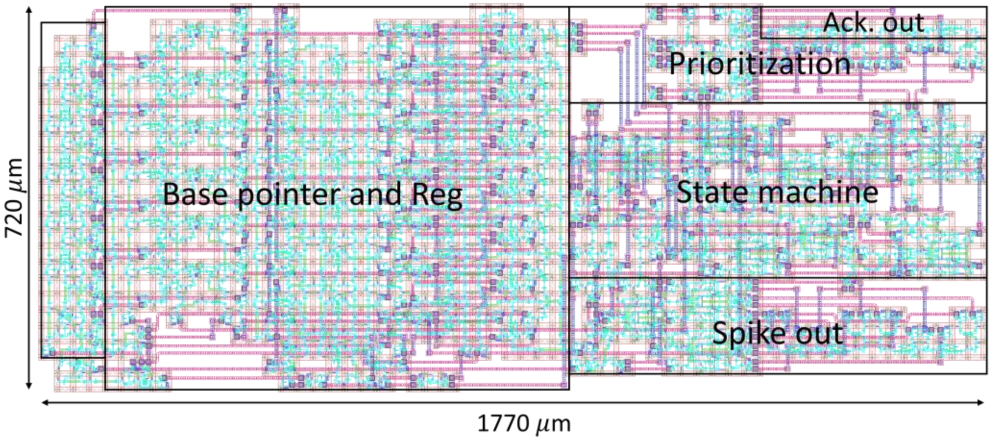
- Measurement process is performed **once every 1 μs**
- Each QECOOL Unit has a **7-bit** buffer to store syndrome values
- If buffer entry size is greater than $K = 3$, QECOOL is performed; otherwise, each Unit waits for measurement process
- MWPM operates with batch-QEC manner

- Threshold value: QECOOL $p = 0.01$, MWPM $p = 0.03$

SFQ implementation of QECOOL decoder



Architecture overview of QECOOL



SFQ design layout of QECOOL Unit

JJs: 3177	Area: 1.274 mm^2	Latency: 215 ps	Power cons.: **2.78 μW**

# of protectable logical qubits on 4-K environment

Suppose $d = 9$, and power budget in 4-K env. is 1 W

$$1_{[W]}/(9 \times 8 \times 2 \times 2.78_{[\mu W]}) = \text{2498 logical qubits}$$

Summary of QECOOL

- Online decoding of surface code in a cryogenic environment is necessary for a scalable superconducting quantum computer
- QECOOL decoder with SFQ implementation is power-efficient and fast to operate in a 4-K environment within code cycle (1 μs)
- QECOOL is capable of decoding a <u>single logical qubit</u> with measurement errors

Requirements for practical decoder

✓ Power consumption
✓ Latency
Functionality
Accuracy

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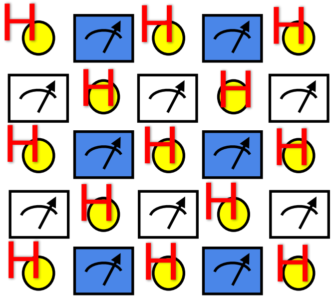
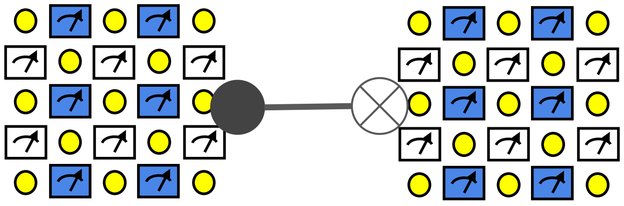
Protecting logical $\{H, \mathrm{CNOT}, T\}$



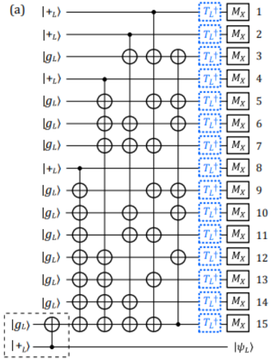
Logical Hadamard

Performed straightforwardly



Logical CNOT

Performed by **Lattice surgery**

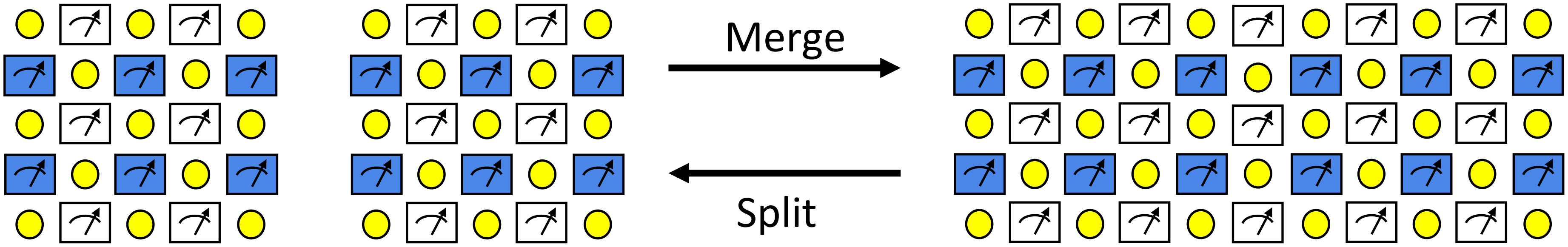


Logical T gate

Performed by **logical *H* and CNOT operations** (+ magic state & gate teleportation)

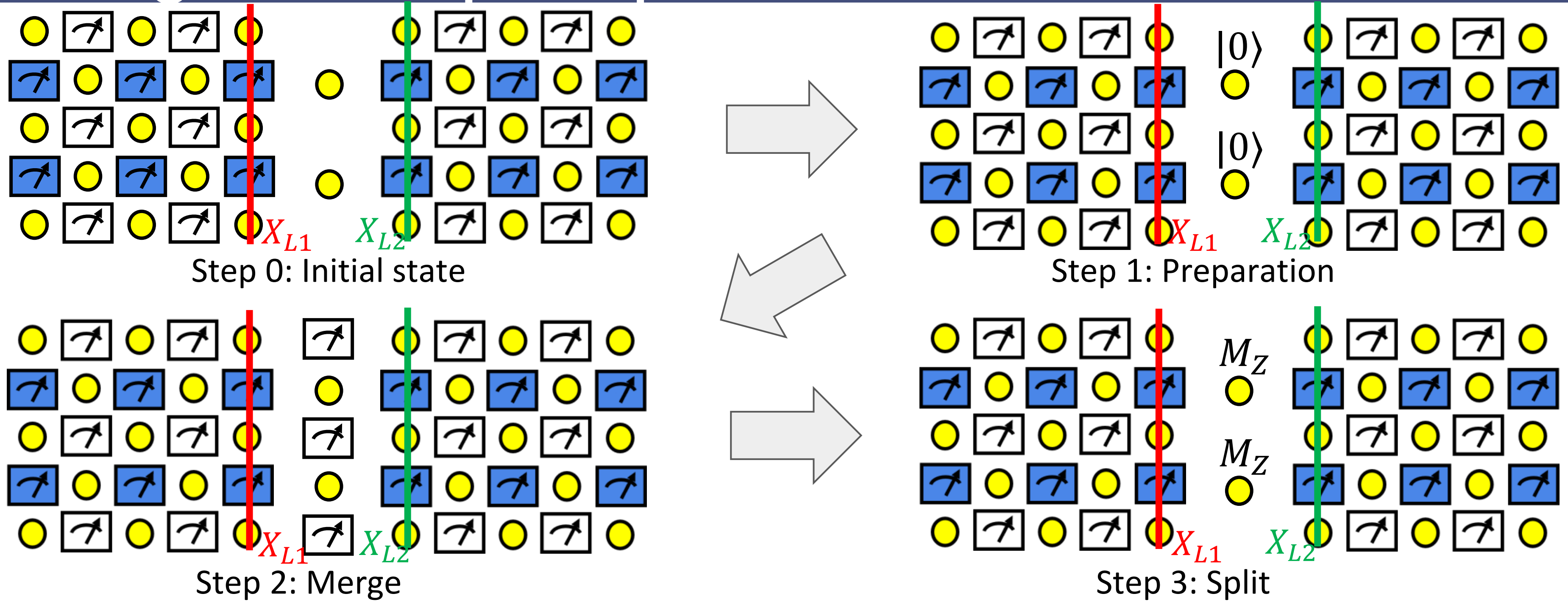
- **Decoding lattice surgery** is essential for fault-tolerant universal quantum computation

Lattice surgery (LS)



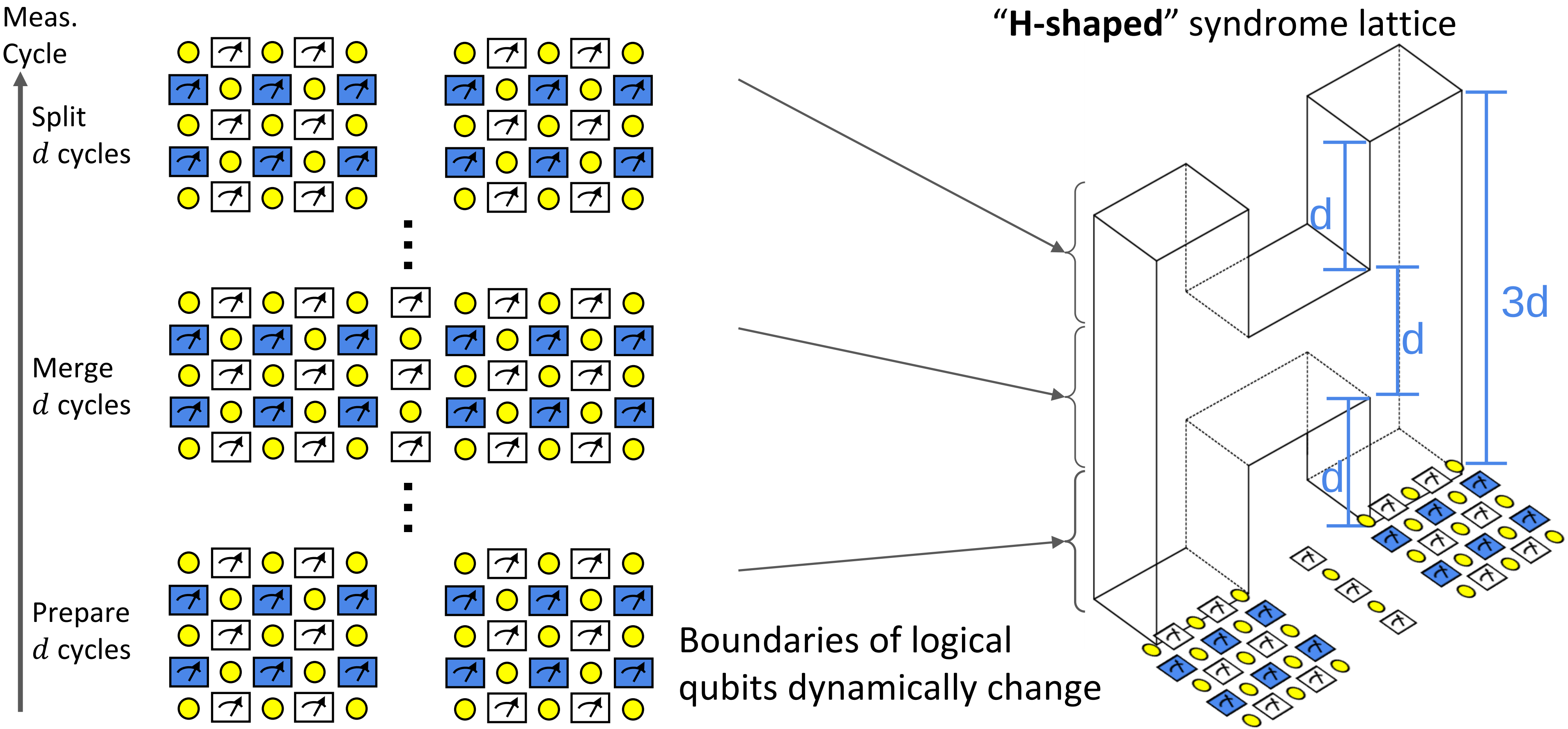
- Framework to perform logical operations with SC-based QEC
- Implement logical Pauli measurements on multiple logical qubits by merging and splitting two of them

Merge and split operation



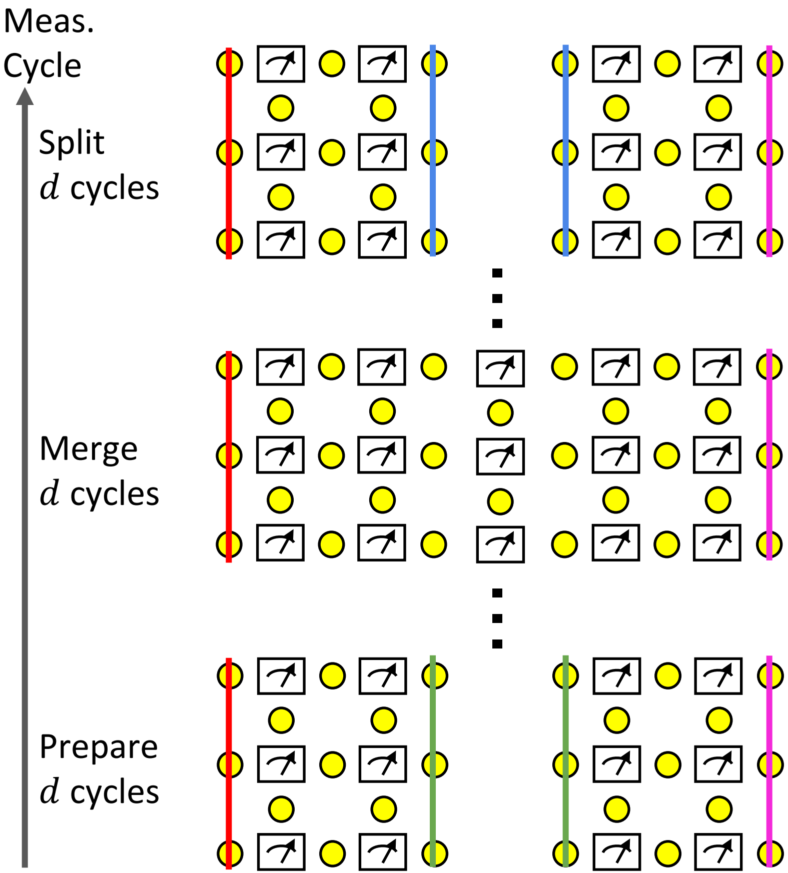
- **Pauli-XX** and **Pauli-ZZ** measurements are realized by merge and split operation
- **Logical CNOT** operation is realized by Pauli-XX and Pauli-ZZ measurements

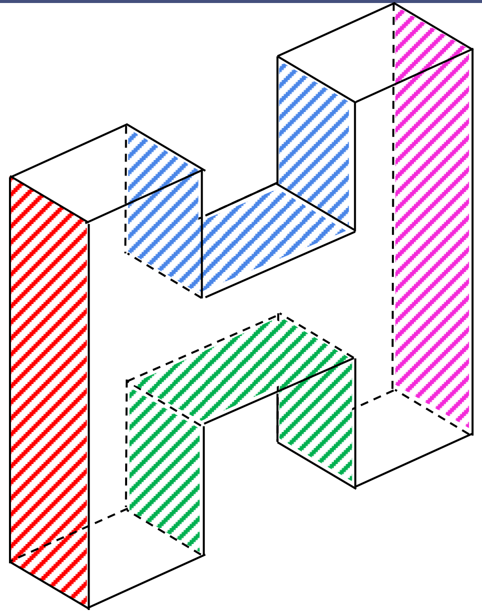
Decoding process of LS



Boundaries of logical qubits dynamically change

X-stabilizer lattice





Boundaries of X-stabilizer lattice

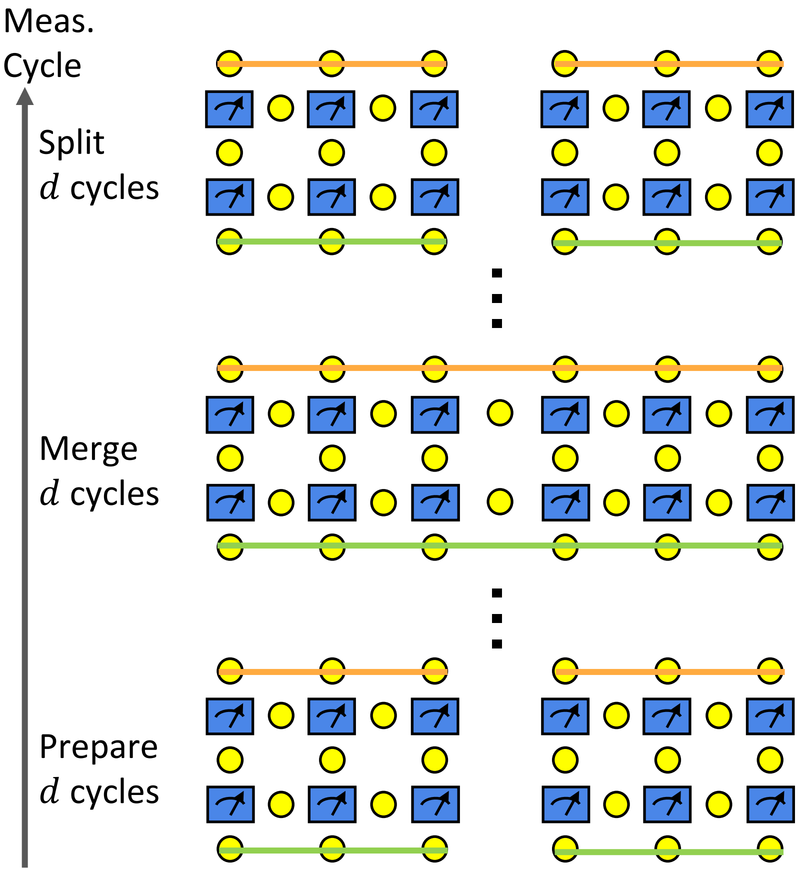
Left - Right: $Z_0 Z_1$ error

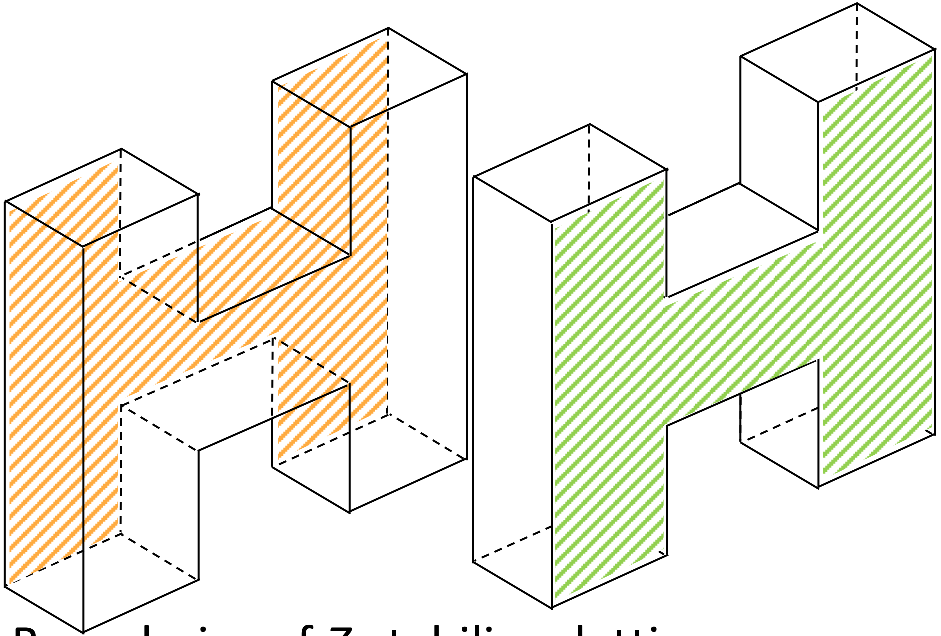
Left - Upper or Lower saddle: $Z_0 I_1$ error

Right - Upper or Lower saddle: $I_0 Z_1$ error

Upper - Lower saddle: Measurement error

Z-stabilizer lattice

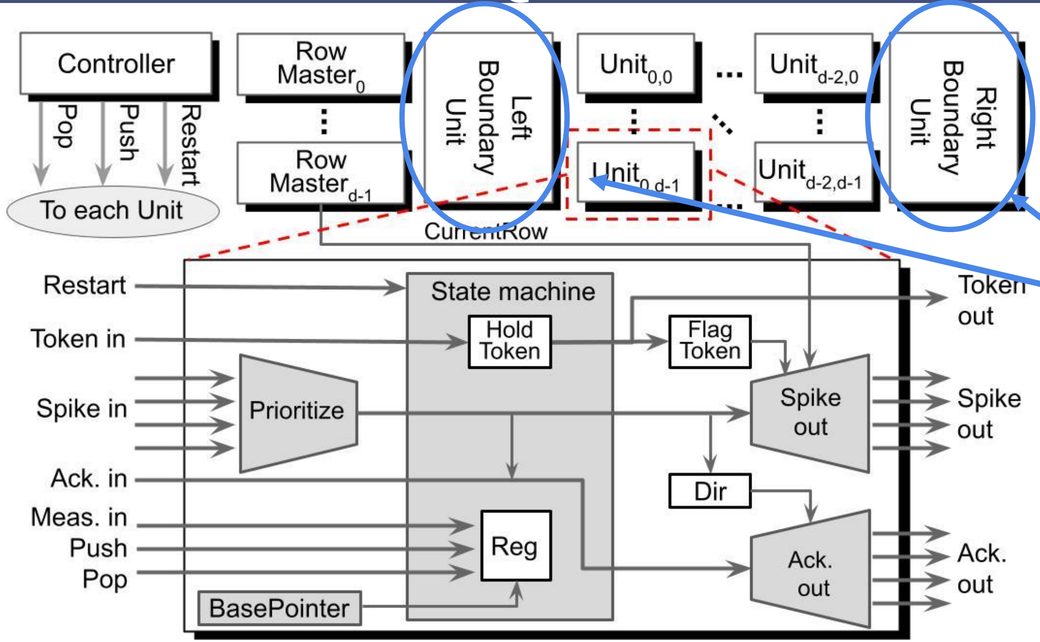




Boundaries of Z-stabilizer lattice

Back - Front: $X_0 = X_1$ error

Limitation of QECOOL



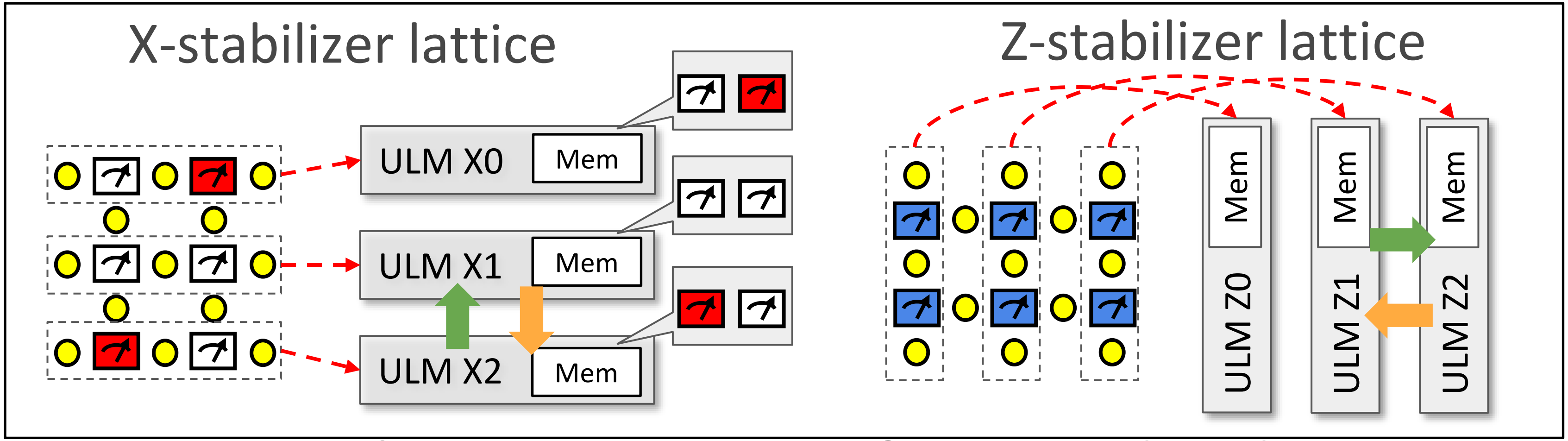
Architecture of QECOOL

<u>Boundary Unit</u>
Hardware modules for boundary matching

- The hardware modules cannot handle dynamic boundary changes required for LS procedures

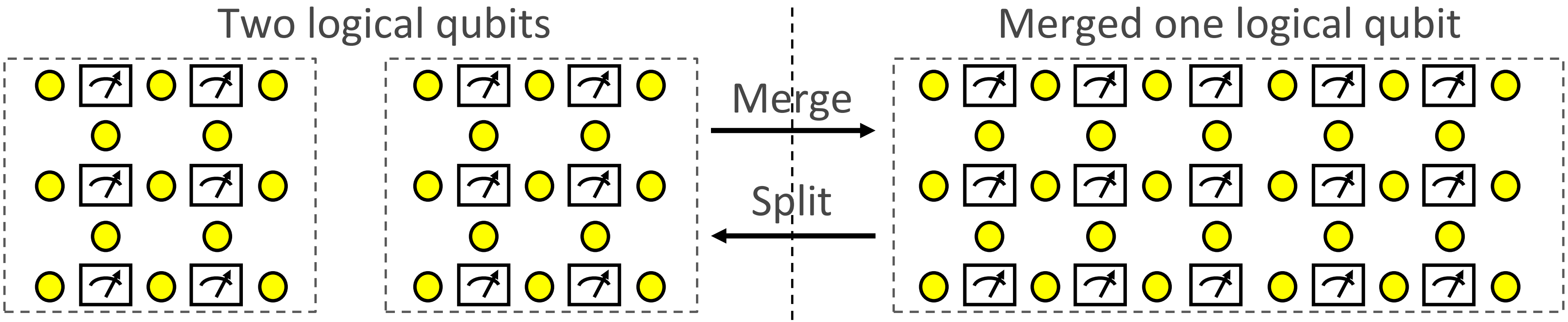
Overview of QULATIS

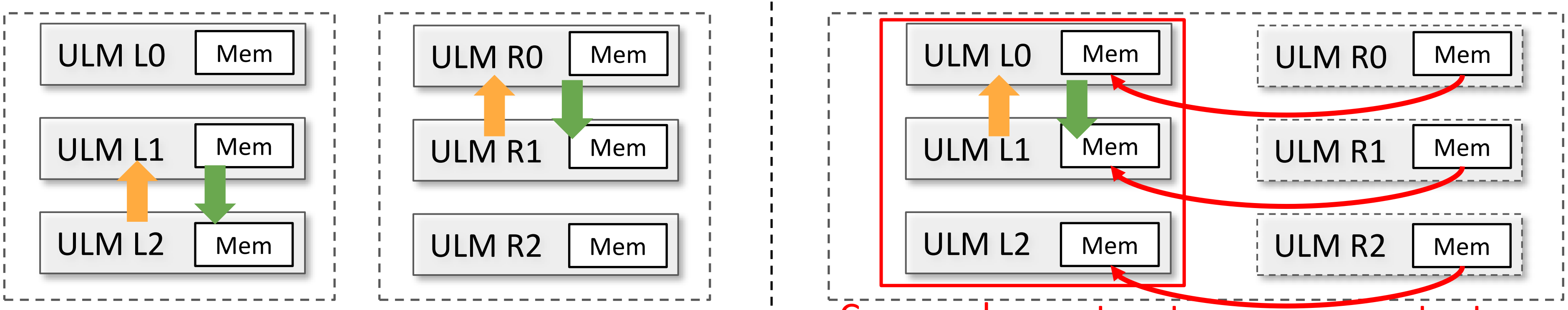
- QUantum error correction methodology toward LATtIce Surgery
- Introduce decoding unit named **united line module (ULM)**
  - Associated with horizontal or vertical line of ancilla qubits
  - Token, Spike and Acknowledge signals between adjacent ULMs to pair hot syndromes



Architecture overview of QECOOL decoder

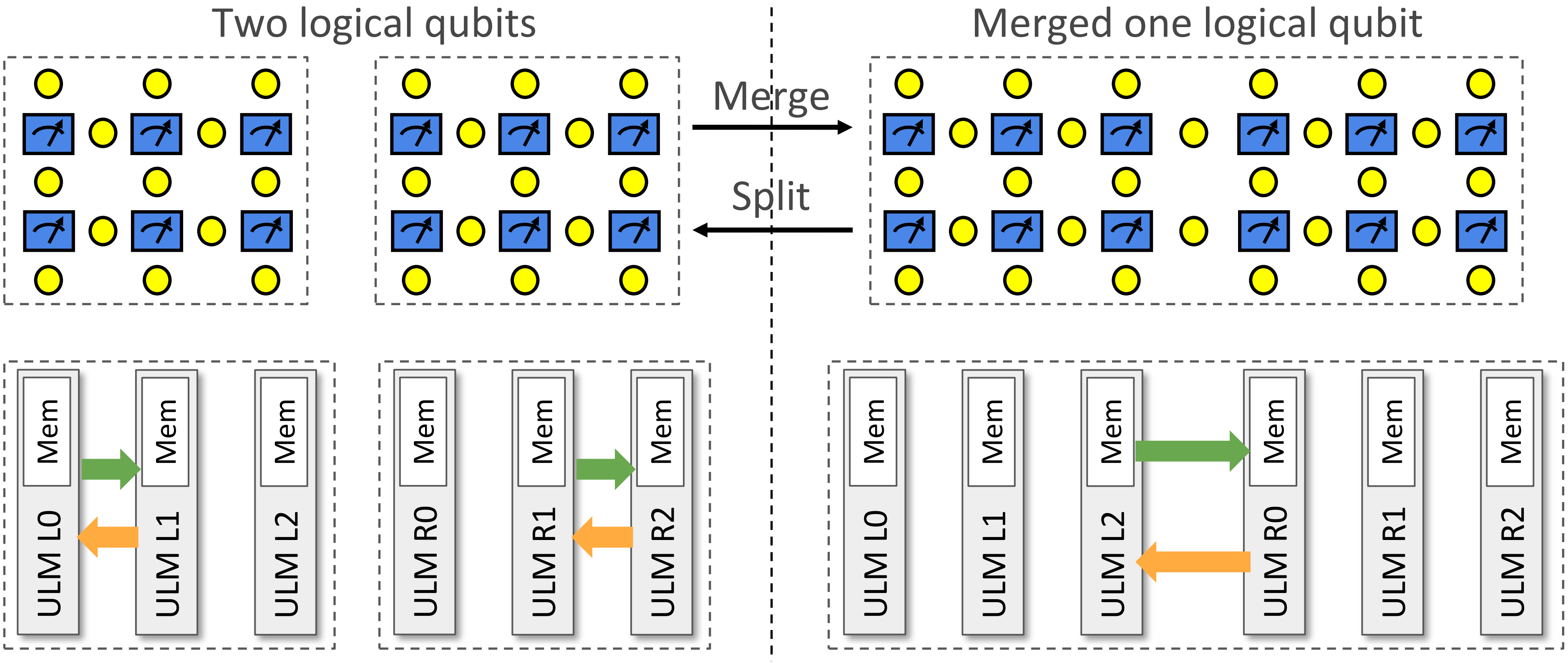
Merge operation of X-stabilizer lattice



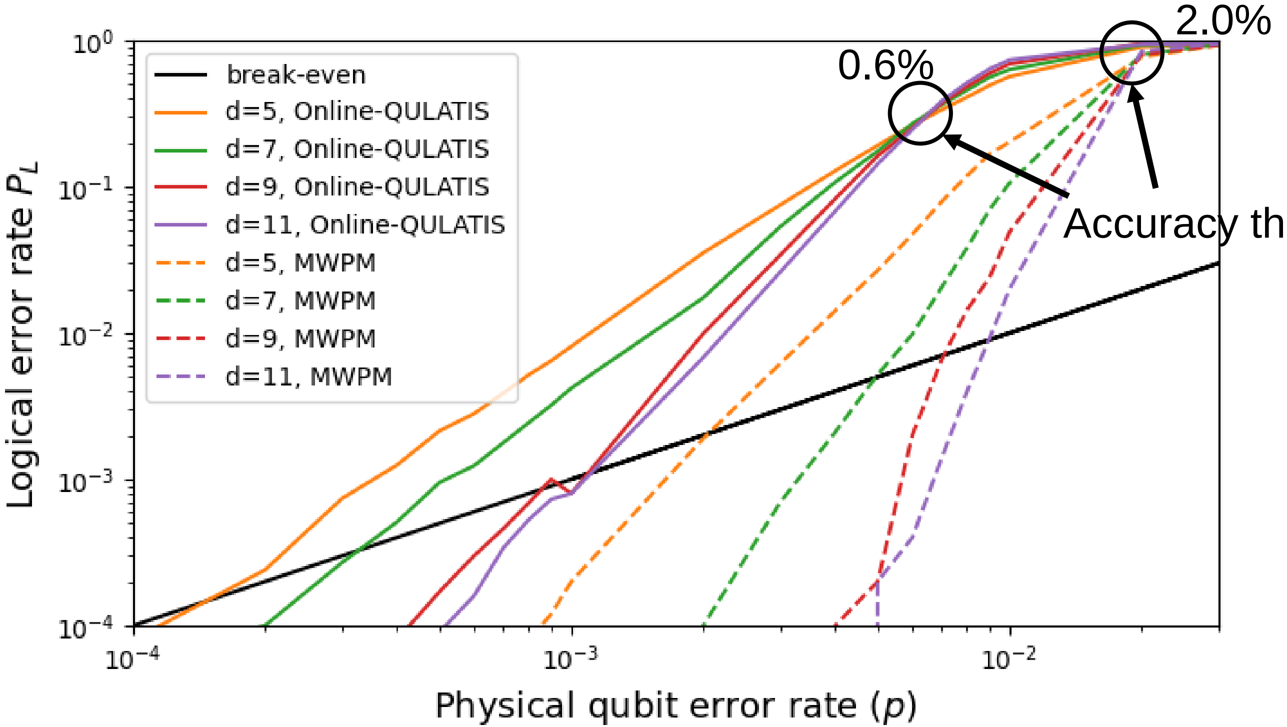


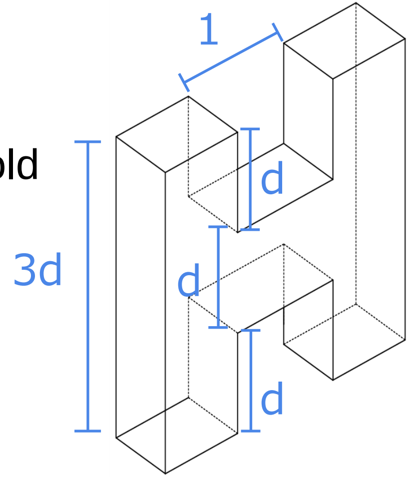
Copy and concatenate memory contents of the right ULMs to the left ones

Merge operation of Z-stabilizer lattice



QEC performance of QULATIS





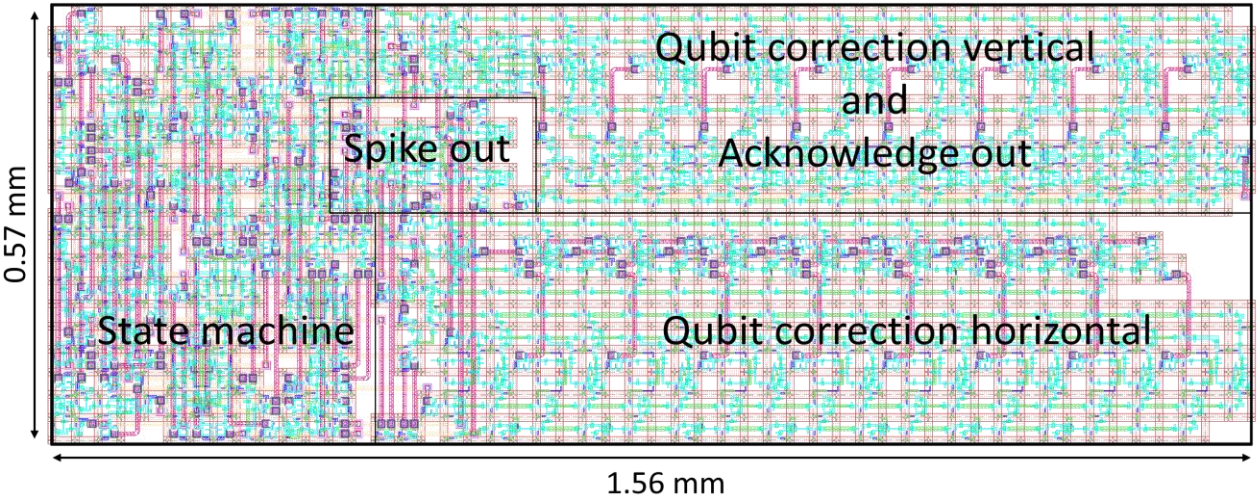
Shape of syndrome lattice

Error model: depolarizing noise model $([I, X, Z, Y] = [1-p, p/3, p/3, p/3])$

MWPM: batch-QEC

QULATIS: online-QEC (buffer size = 7, operating frequency = 2 GHz)

SFQ design of ULM



SFQ design of ULM
except memory module

Total : 2412 JJs
Area: 0.889 mm^2
Latency: 157.5 ps
Power : **2.07 μW** @2 GHz

- Memory module is assumed to be a 64-kb hybrid SFQ-CMOS memory array proposed by Van Duzer et al.[4]
  - Readout delay 400 ns, power 12 mW@1 GHz, 4 K
- **2395** distance-9 logical qubits can be protected in a cryogenic environment in terms of power consumption

[4] Theodore Van Duzer, Lizhen Zheng, Stephen Whiteley, Hoki Kim, Jaewoo Kim, Xiaofan Meng, and Thomas Ortlepp. 64-kb hybrid Josephson-CMOS 4 Kelvin RAM With 400 ps access time and 12 mW read power. IEEE Transactions on Applied Superconductivity, vol. 23, no. 3

Summary of QULATIS

- Lattice surgery and its decoding are essential for fault-tolerant universal quantum computation
- We propose QULATIS to decode lattice surgery
  - Accuracy threshold value: 0.6% for merge-and-split operation
- We design superconducting decoder based on QULATIS
  - 2395 logical qubit can be protected in a cryogenic environment

Requirements for practical decoder

✓ Power consumption

✓ Latency

✓ Functionality

Accuracy

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Summary

- Online decoding of surface code in a cryogenic environment is necessary for a scalable superconducting quantum computer
- **QECOOL** decoder is power-efficient enough to protect around 2500 logical qubits with distance-9 SC in a cryogenic env.
- **QULATIS** is an extension of QECOOL, which supports logical operations via lattice surgery
- Accuracy of QECOOL and QULATIS is lower than MWPM due to its greedy and online nature
  - **NEO-QEC**: Extension of QECOOL/QULATIS with binarized NN for better accuracy (arXiv:2208.05758)