Toward System-Level Optimization of Superconducting Quantum Computers: The Case of QAOA

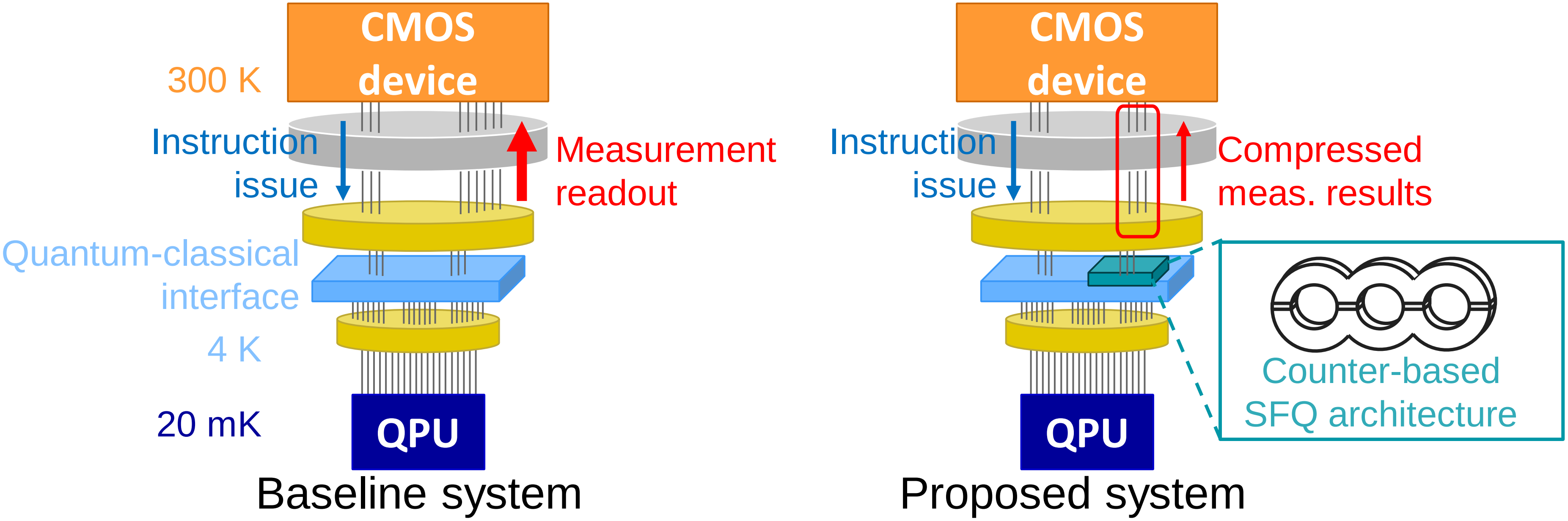
RIKEN Center for Quantum Computing

Special Postdoctoral Researcher

Yosuke Ueno

This talk is based on arXiv.2023.01630

Summary of this talk

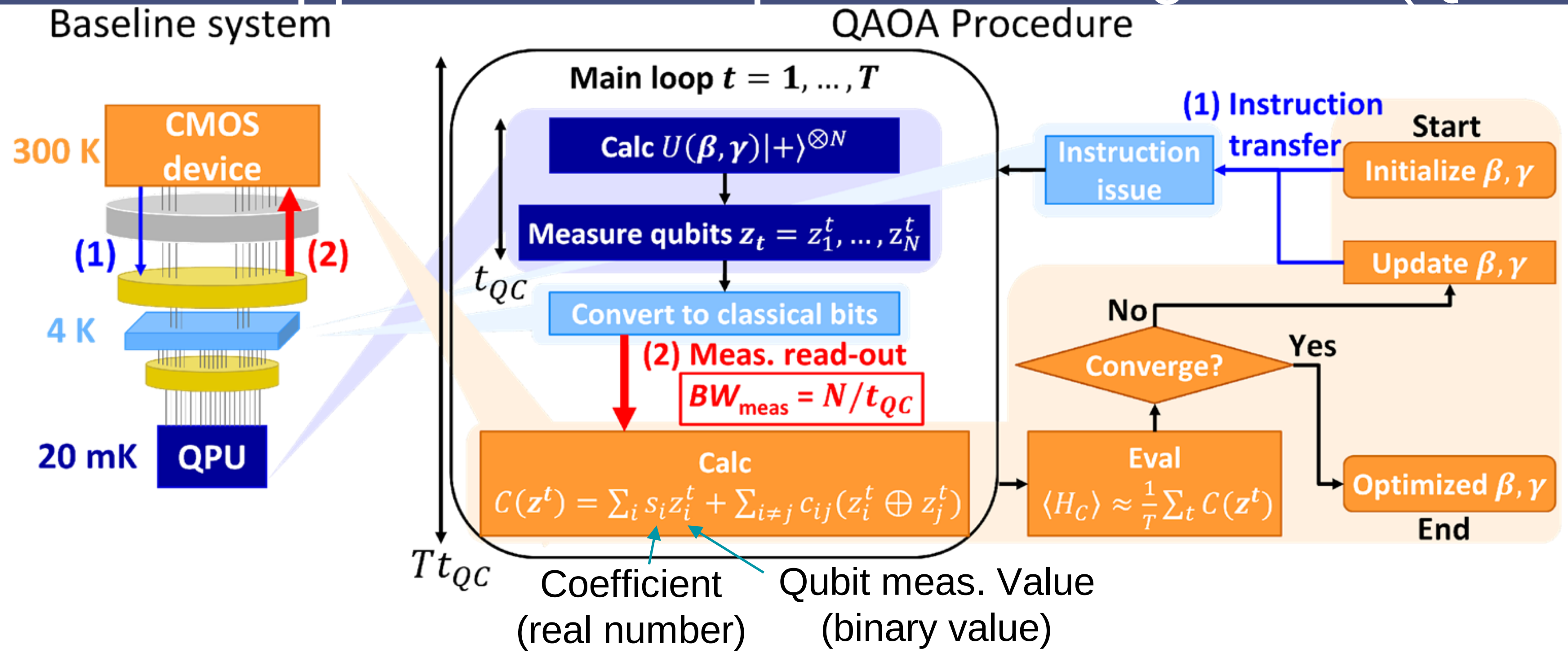


- Cryogenic quantum machine requires many inter-temperature cables
  - Hardware complexity, heat inflow, peripheral power etc.
- For QAOA, measurement readout communication is dominant
- Counter-based SFQ architecture reduces meas. bandwidth

Contents

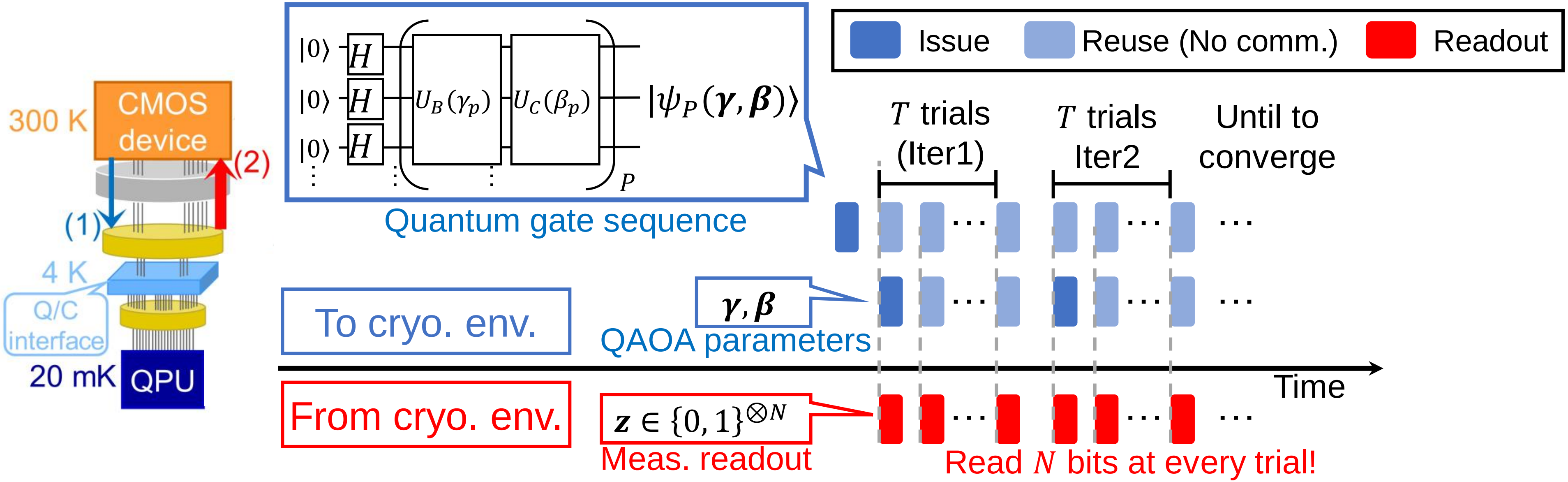
- Quantum approximation optimization algorithm (QAOA)
- Bandwidth modeling of cryogenic QAOA machine
- Measurement bandwidth reduction by counter-based calculation
- Evaluation: bandwidth v.s. power dissipation in cryostat
- Summary and future work

Quantum Approximation Optimization Algorithm (QAOA)



- One of the simplest NISQ applications
- QAOA require inter-temperature communication for (1) instruction issue and (2) qubit measurement readout

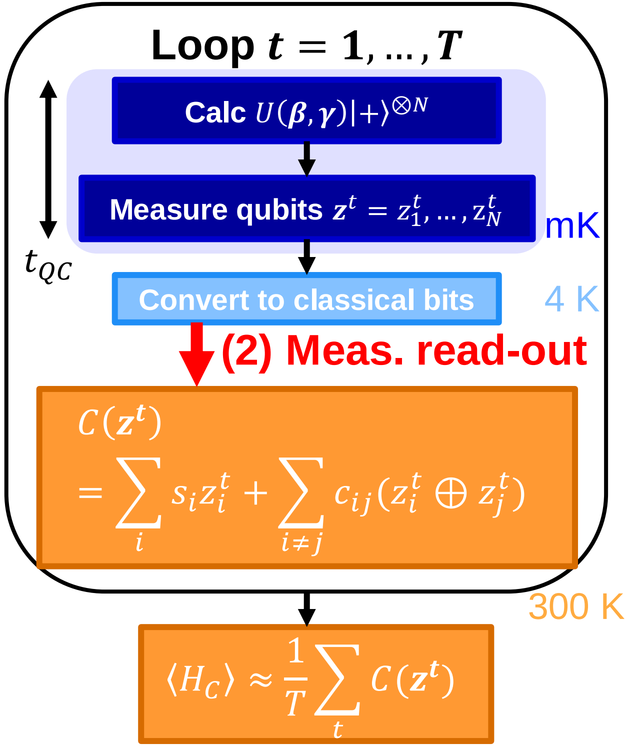
Inter-temperature communication timing of QAOA



- Gate sequence is reused throughout QAOA computation
- QAOA parameters are reused through T trials (1 iteration)
- *N*-bit measurement readout is transferred after every trial
  - This is bottleneck! We focus on the measurement bandwidth

Expectation value calculation using counters

Conventional calculation of QAOA



Expectation value

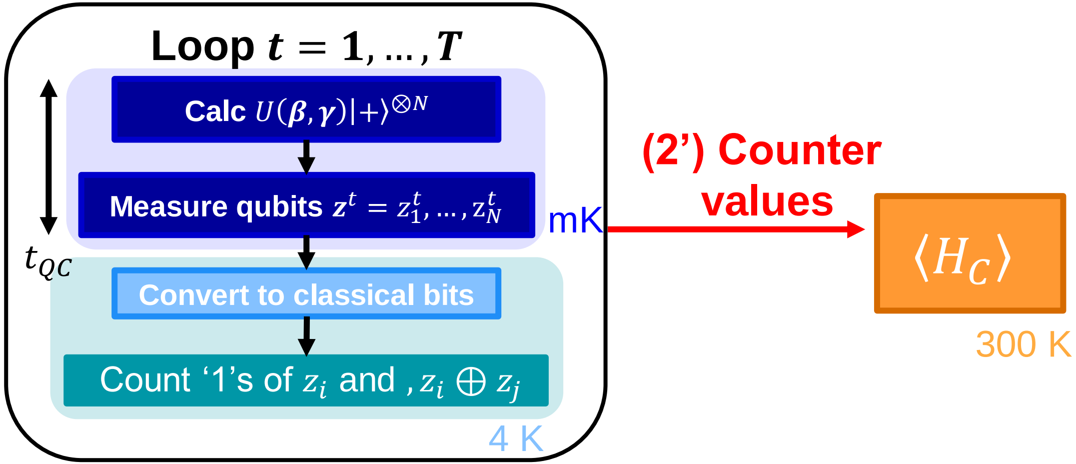
Counter-based calculation of QAOA

Deformation of exp. value calc.

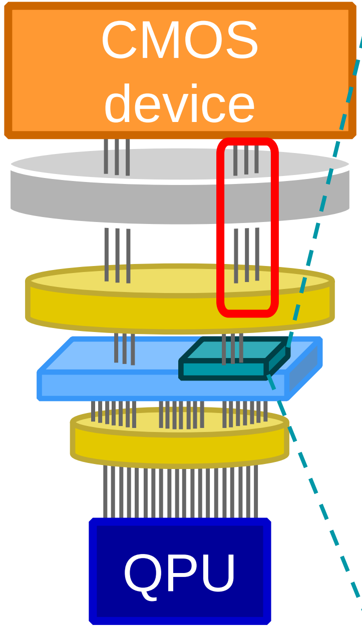
$$\langle H_C \rangle \approx \frac{1}{T} \sum_t C(z^t)$$

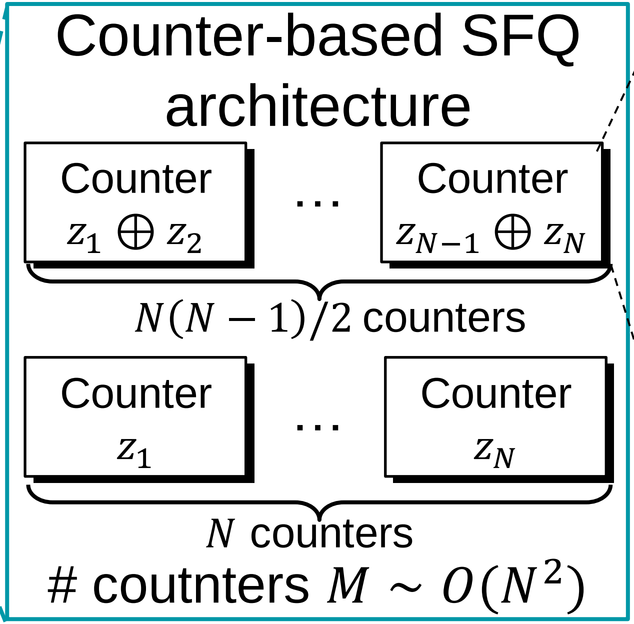
$$= \frac{1}{T} \left(\sum_i s_i \sum_t z_i^t + \sum_{i \neq j} c_{ij} \sum_t (z_i^t \oplus z_j^t) \right)$$

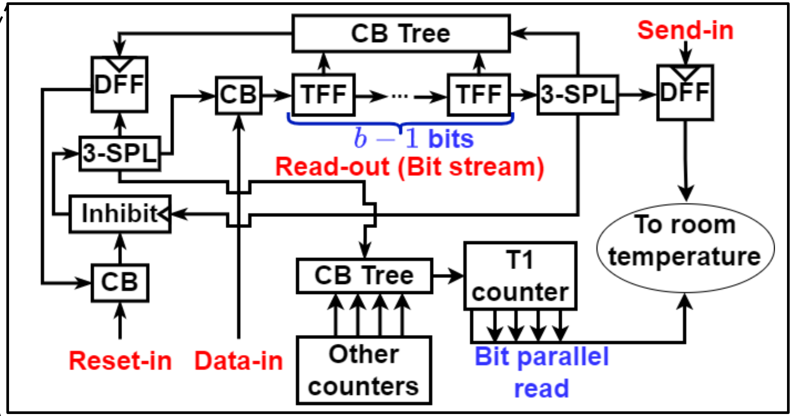
Count of '1's of z_i **Count** of '1's of $z_i \oplus z_j$



Counter-based architecture design







Each counter
JJs : 11b+31
Power : 9.71b+16.8 (pW)

- Bandwidth is reduced by factor of 2^b with b-bit counters
  - By sending only MSB after counter overflow
- Each counter has ten picowatt orders of power
  - when applied ERSFQ (1.3MHz operating frequency)

Bandwidth and power dissipation in cryogenic env.

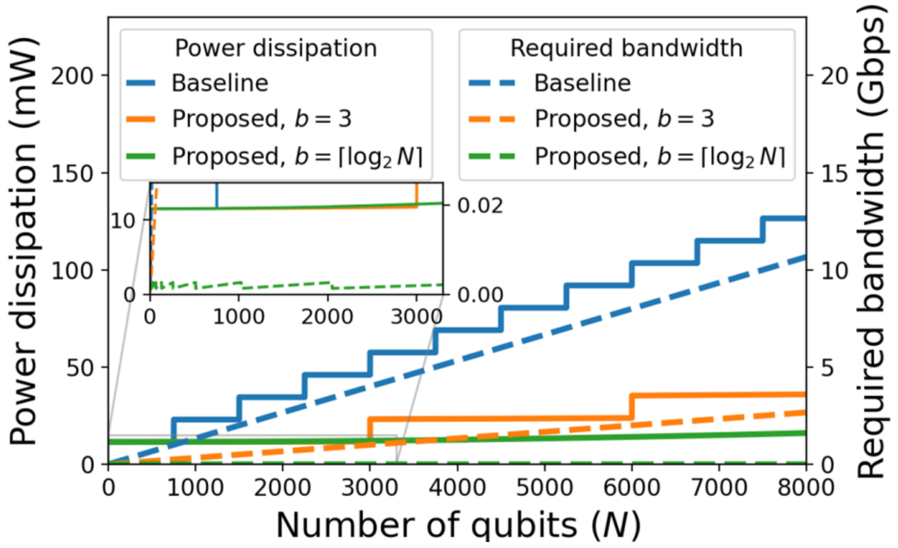


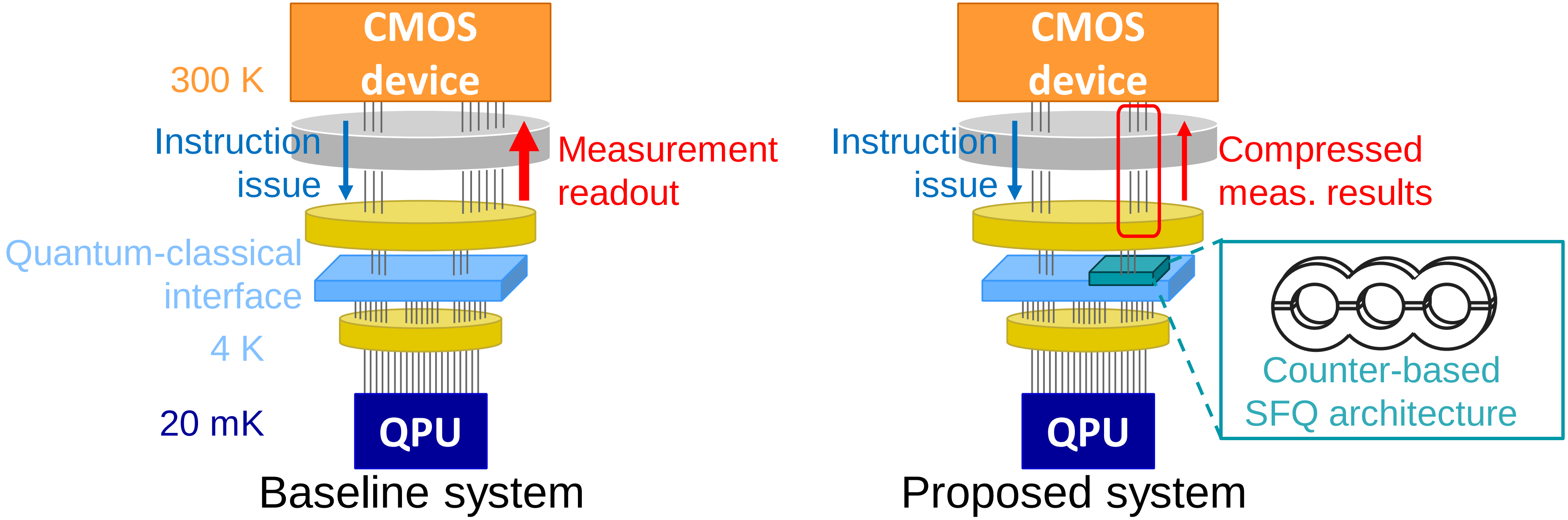
TABLE I: Configuration of cables and SFQ counters

	Power dissipation	Configuration
Coaxial cable	Heat inflow: 1.0 mW[10] Periphelars: 10.5 mW[10]	One cable per 1 Gbps
SFQ counter	$(9.71b + 16.8)$ pW	$M = N(N+1)/2$ ERSFQ (Freq. = 1.33 MHz)

[10] S. Krinner et al., "Engineering cryogenic setups for 100-qubit scale superconducting circuit systems," EPJ Quantum Technol., vol. 6, no. 1, p. 2, 2019

- Bandwidth is exponentially reduced to counter bitwidth b
  - Setting b to $O(\log N)$ keep bandwidth constant
- Our architecture reduced # of cables, which leads to power consumption and heat inflow reduction in cryogenic env.

Summary and future work



- Counter-based SFQ architecture reduces meas. bandwidth during QAOA
- First step in system-level optimization based on application characteristics of quantum computers
- Future work: extend the method to VQE or other VQAs